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INTERFACE

CX20810/CX20811 High-Definition Voice Capture IC Datasheet

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Overview

The Synaptics CX20810/CX20811 device family is a high performance analog front-end, HD voice capture IC for voice recognition, control, and conferencing applications. The devices support microphone array with up to four synchronized ADCs and programmable pre-amplifiers. Each pre-amplifier has a dedicated micbias supply to eliminate crosstalk. The entire input path guarantees a 106dB dynamic range that allows the voice system to use the full performance of a high SNR microphone using a low microphone boost, which prevents microphone saturation issues. This range is critical for far field conditions, and also ideal for compact speakerphone designs where the microphone and speakers are in close proximity.

The CX20810/CX20811 device family features high resolution digital and analog gain control over a wide range, allowing a select optimum operating point for microphones with a wide range of sensitivity. The smooth gain ramping circuit allows for dynamically adjusting microphone gain without introducing audible artifacts.

A mono digital PWM Class-D amplifier is only available on the CX20811 device, and can be used for the ringer and audio playback functions. The Class-D amplifier output drives up to $1W_{rms}$ into a 4Ω load. The PWM output can be configured to support an external output stage amplifier for higher output power applications.

The CX20810/CX20811 device family is the industry's first dedicated voice capture IC designed to service the most demanding voice interactive applications.

CX20810/CX20811 Features

Voice Coder-Decoder (VC)

- ADC features:
 - Four high performance ADCs with programmable pre-amplifiers
 - Power consumption per ADC—10mA
 - Differential or SE ADCs
 - ADC channels mixer
 - ADC audio performance:
 - Dynamic range = 106dB
 - THD+N = –85dB at –1dBFS
- Microphone or line input support
- Audio sample rates supported:
 - 8kHz
 - 16kHz
 - 22.05kHz
 - 24kHz
 - 32kHz
 - 44.1kHz
 - 48kHz
 - 88.2kHz
 - 96kHz
- Four micbias, one for each of the four ADCs—supported voltage is 1.5V to 4V
- Programmable pre-amplifier with integrated analog and digital gains:
 - Analog gain = 0dB to 30dB with 0.5dB steps
 - Digital gain = –74dB to 12dB with 0.125dB steps

- Smart gain controller adjusts the gain in both analog and digital to allow high dynamic range at different gains
- Zero crossing detection minimizes audible artifacts when gain switching
- Integrated offset calibration
- Four programmable biquads to configure Q-notches, HPFs, or other type of filters

Control Interfaces

I²C slave:

- Two-wire serial control interface
- I²C clock frequency support from 100kHz up to 400kHz
- Addressing is 8-bit
- Register width is 8-bit

Digital Audio Interface

- I²S features:
 - Supports configurable I²S/Pulse Code Modulation (PCM) audio data interfaces multiplexed on common lines
 - Default configuration is I²S
 - Four-wire audio I²S/PCM output supporting the four ADCs
 - (CX20811 only) Three-wire audio I²S/PCM input that supports the mono Digital-to-Analog Converter (DAC) that drives the PWM
- Supports master and slave configuration
- Supported sample rates:
 - 8kHz
 - 16kHz
 - 24kHz
 - 32kHz
 - 44.1kHz
 - 48kHz
 - 96kHz
- Supported sample widths:
 - 8-bit
 - 16-bit
 - 24-bit
- Supported modes:
 - I²S
 - Left-justify
 - Right-justify
 - Digital Signal Processor (DSP)/PCM

Clocking

- Integrated Phase Locked Loop (PLL) is derived from MCLK
- Integrated PLL input clock supports:
 - Master mode = 900kHz up to 50MHz
 - Slave mode = $256 \cdot F_s$

General

- Configurable low-power and high performance modes
- Integrated Low Dropout (LDO) linear regulator that allows a single supply (3V~5.5V)
- Integrated Charge Pump (CP) for power management
- Four General Purpose Input/Outputs (GPIOs)
- Support of 1.8V and 3.3V digital Input/Outputs (I/Os)

Playback Audio (Only Supported on the CX20811)

- Mono digital PWM Class-D amplifier
- Class-D amplifier outputs up to 1W into 4Ω speakers
- Audio sample rates supported:
 - 8kHz
 - 16kHz
 - 22.05kHz
 - 24kHz
 - 32kHz
 - 44.1kHz
 - 48kHz
 - 88.2kHz
 - 96kHz

Footprint

- CX20810-11Z—6mm x 6mm, 48-pin Quad Flat No-leads (QFN)
- CX20811-11Z—7mm x 7mm, 60-pin QFN
- CX20811-15Z—3.280mm x 3.580mm, 0.4mm pitch, 0.26mm ball size, 58-ball Wafer-Level Chip Scale Package (WLCSP)

Applications

- Voice conferencing systems
- Voice interactive products
- Audio capture
- IVI

Hardware Interface

Block Diagrams

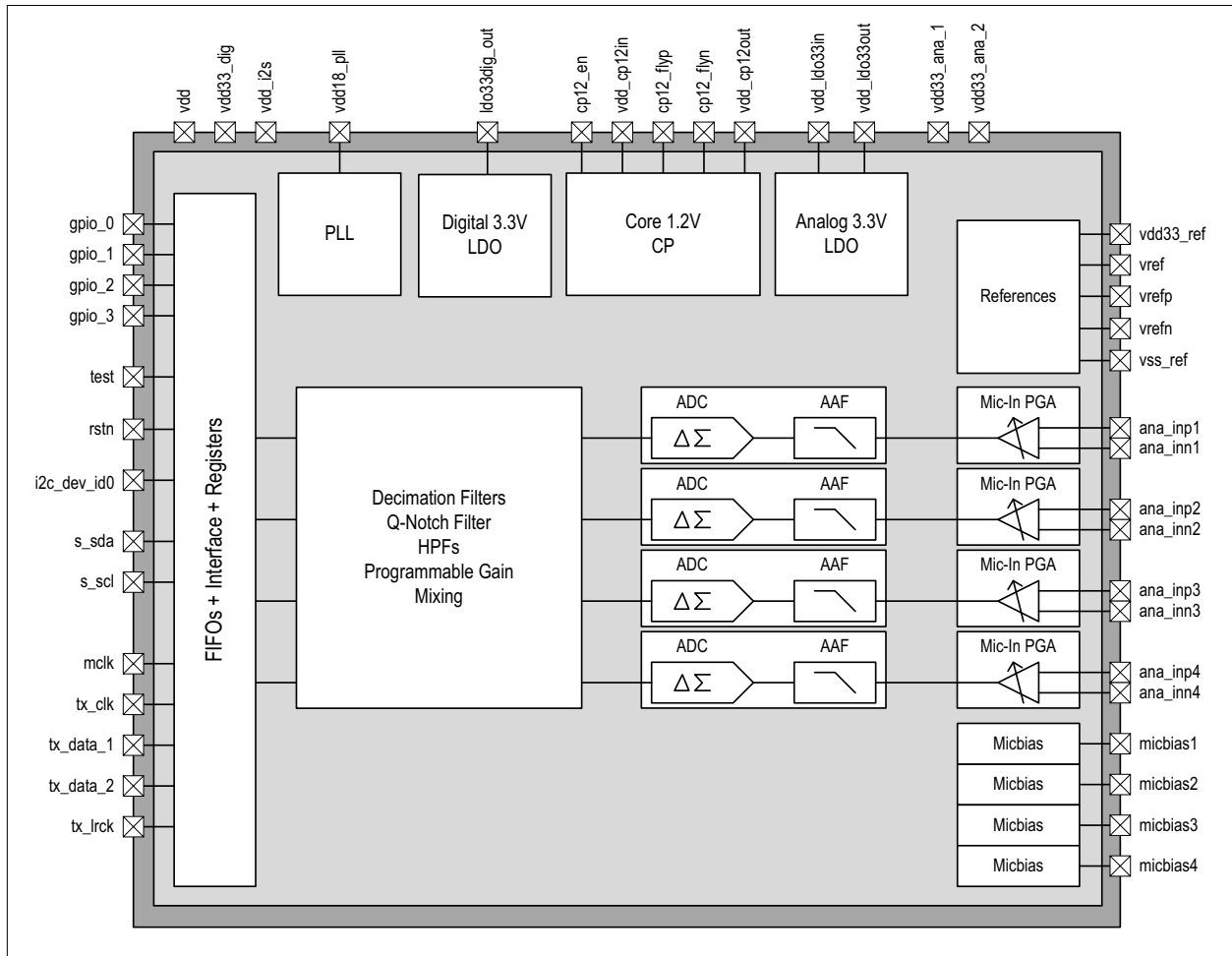


Figure 1: CX20810-11Z Block Diagram

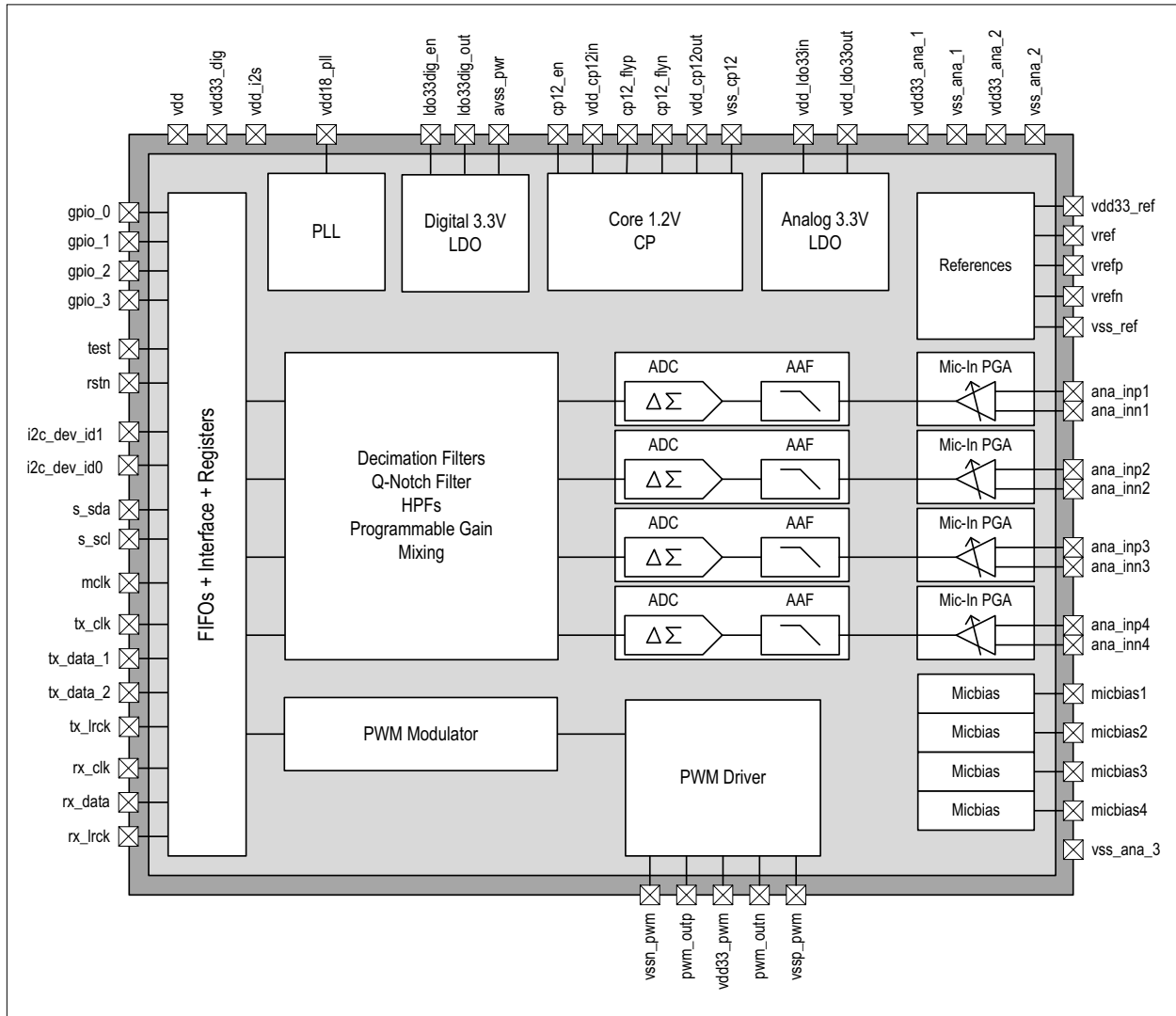


Figure 2: CX20811-11Z Block Diagram

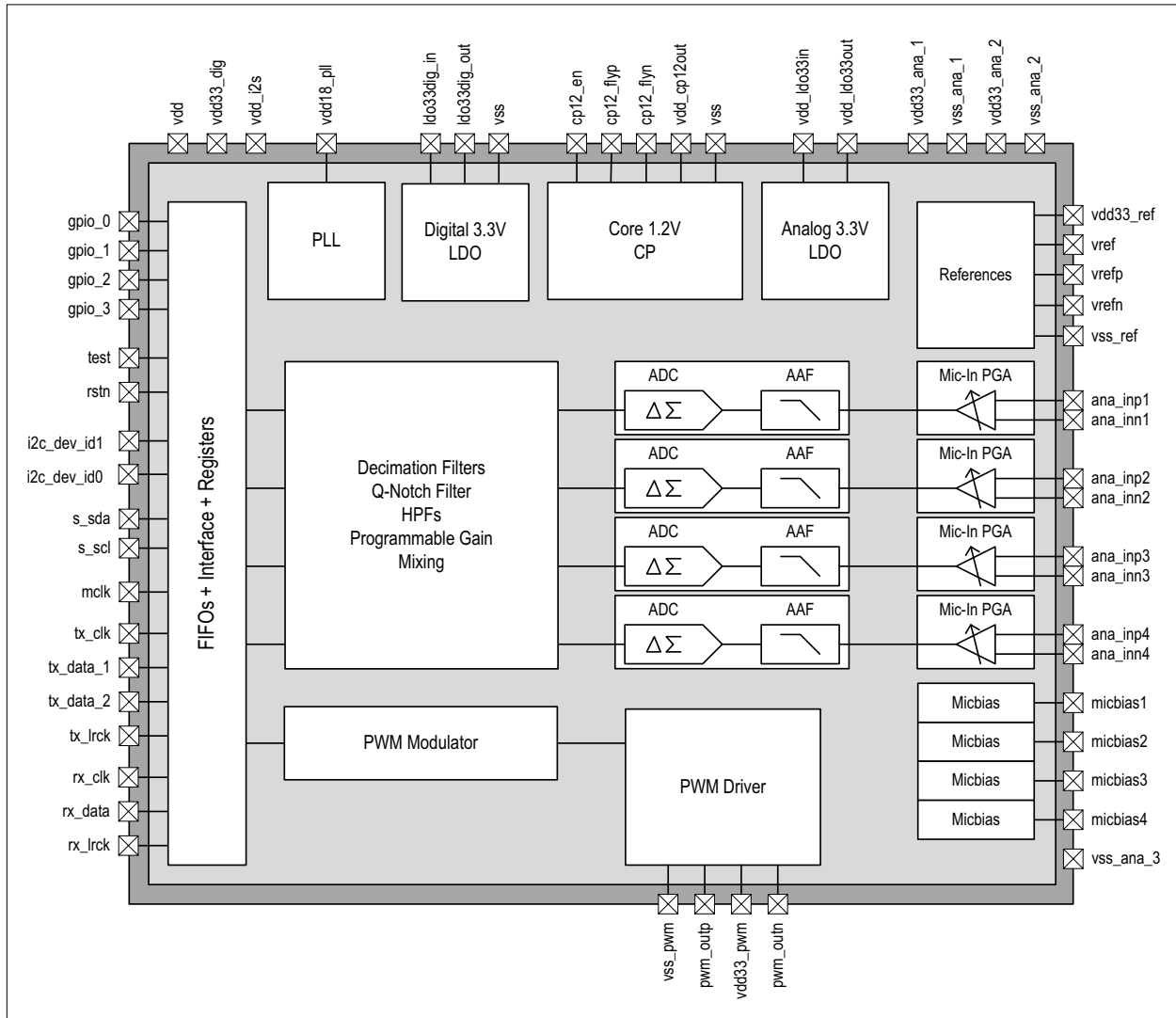


Figure 3: CX20811-15Z Block Diagram

Pin Configuration

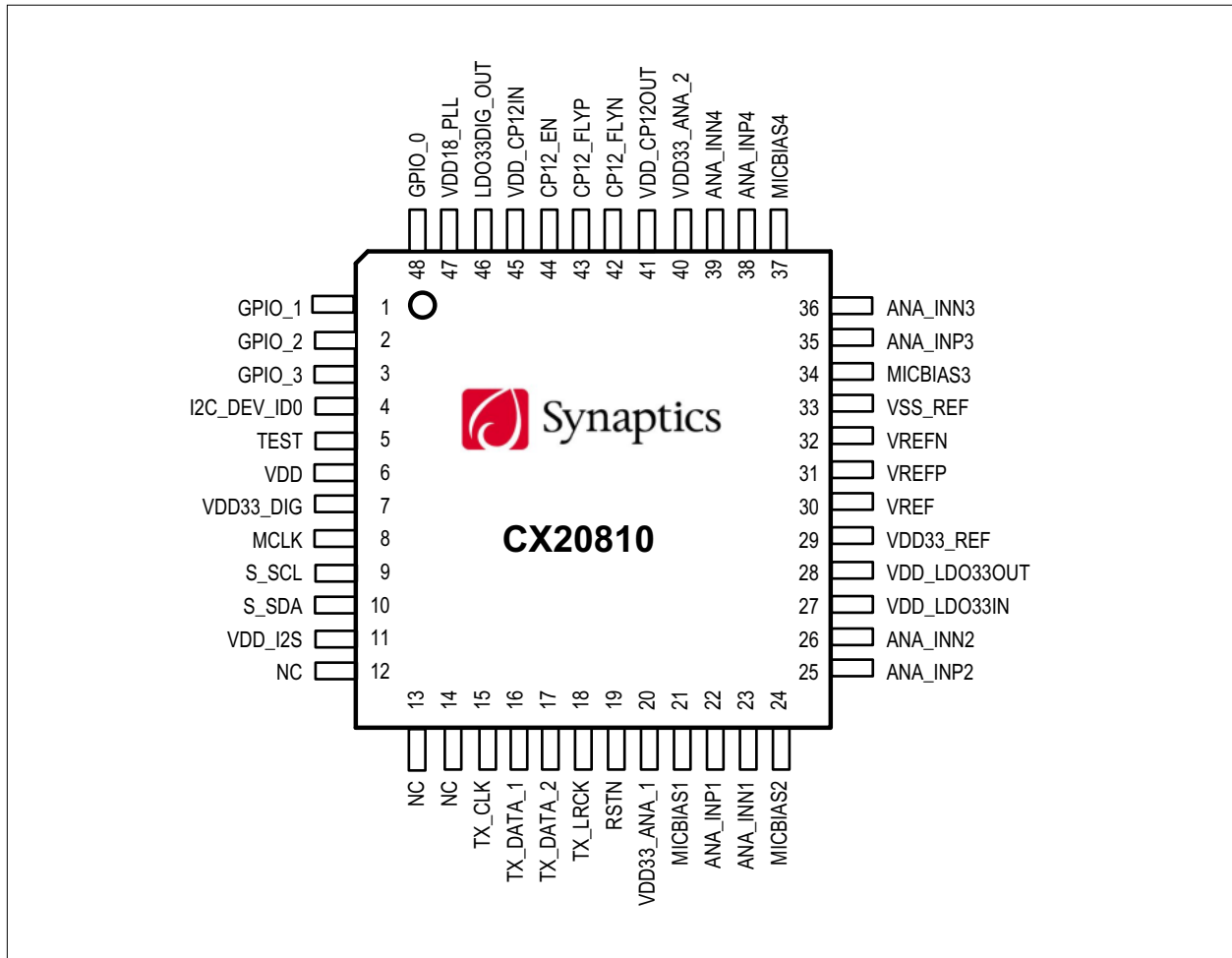


Figure 4: CX20810-11Z Pin Configuration

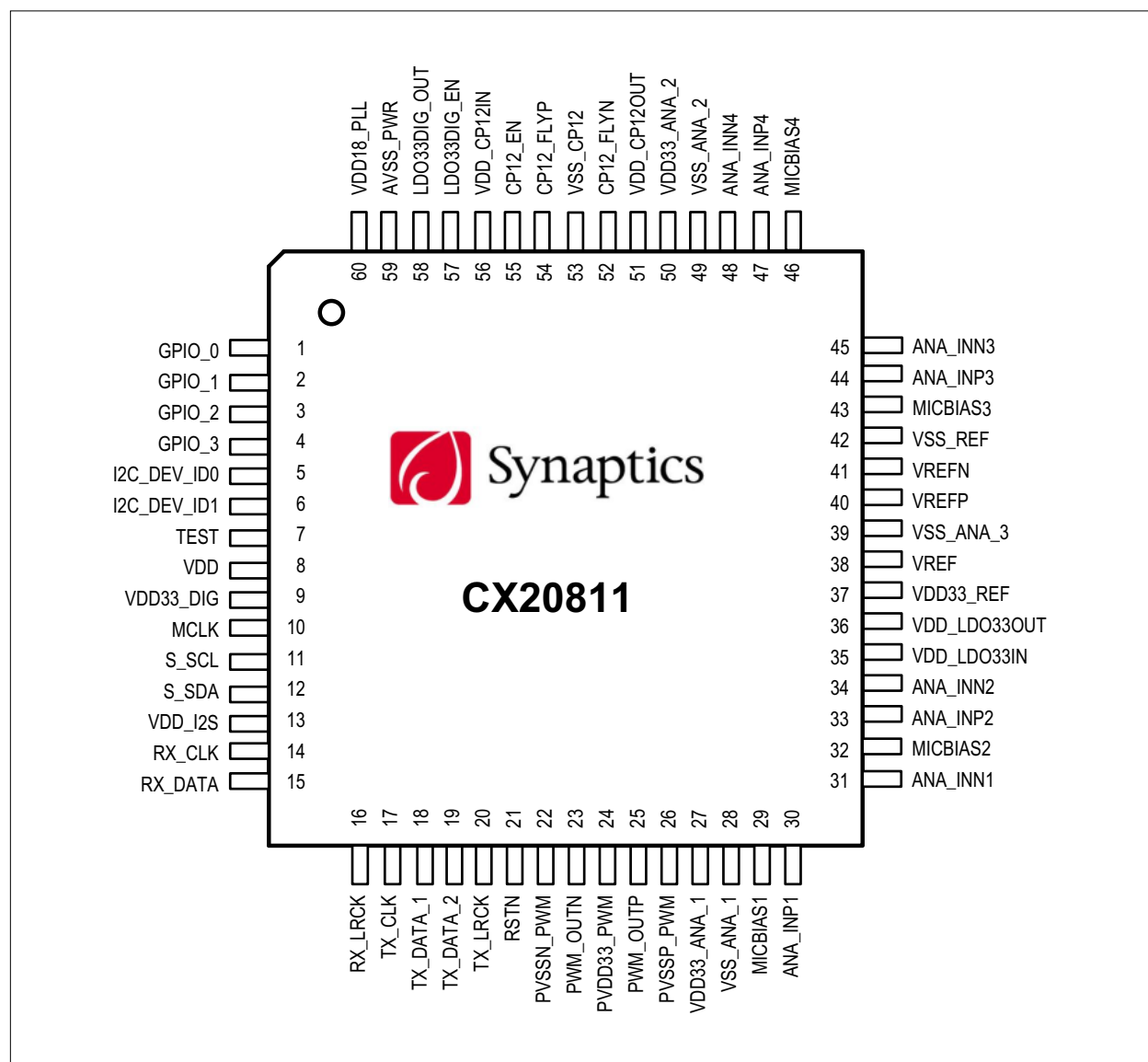


Figure 5: CX20811-11Z Pin Configuration

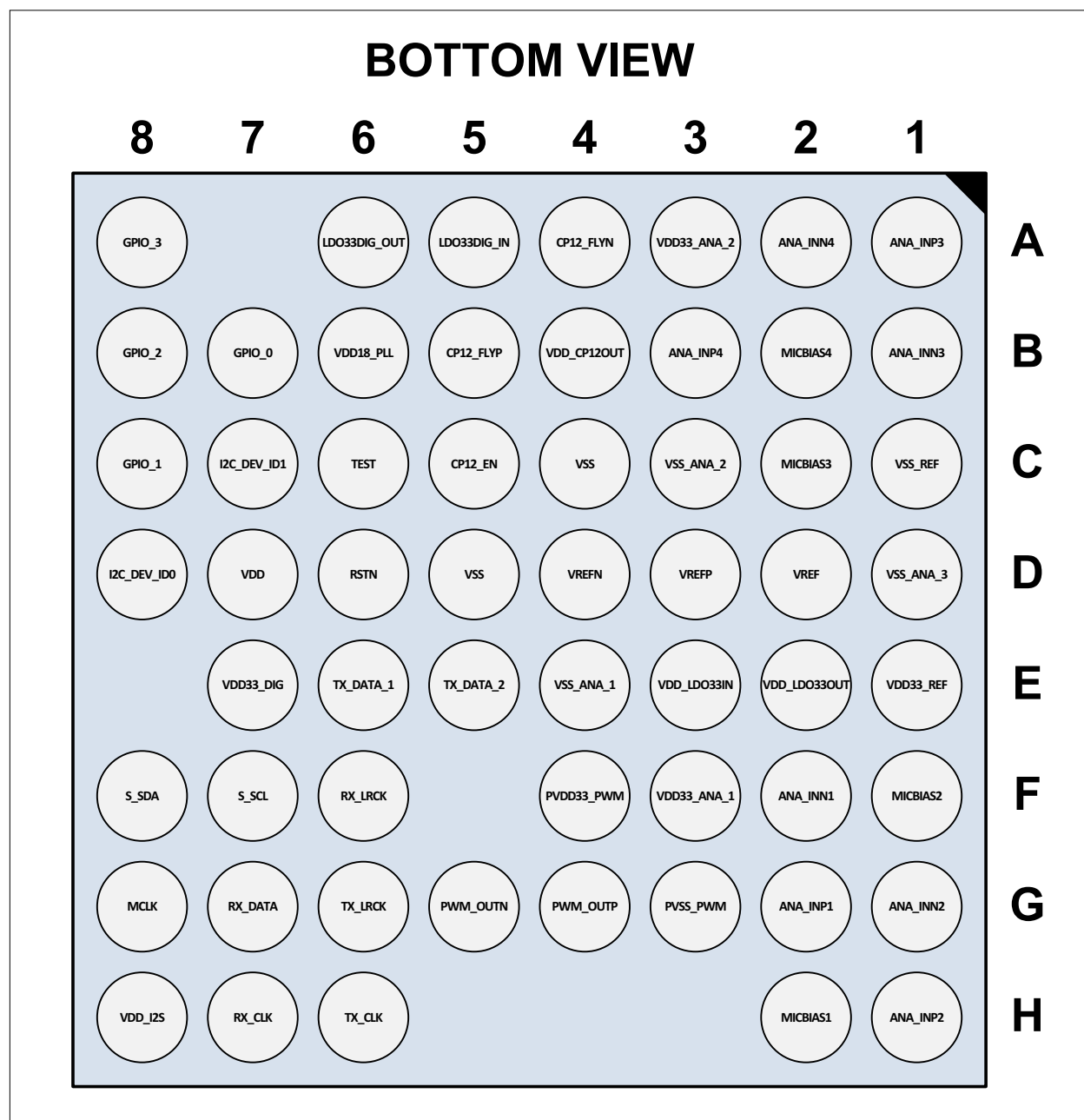


Figure 6: CX20811-15Z Pin Configuration

Signal Definitions

The following lists the acronyms used in Table 1:

- GND = Ground
- I = Input
- Ia = Input analog
- Id = In Digital
- I/O = Input/Output
- O = Output
- Oa = Output analog
- PWR = Power

Table 1: Pad Signal Definitions

Pin Label	Pin Number			I/O Type	Signal Name/Description
	CX20810-11Z	CX20811-11Z	CX20811-15Z		
General GPIO					
GPIO_0	48	1	B7	Digital I/O	GPIO. Programmable pull-up and drive control has an internal pull-down.
GPIO_1	1	2	C8	Digital I/O	GPIO. Programmable pull-up and drive control has an internal pull-down.
GPIO_2	2	3	B8	Digital I/O	GPIO. Programmable pull-up and drive control has an internal pull-down.
GPIO_3	3	4	D8	Digital I/O	GPIO. Programmable pull-up and drive control has an internal pull-down.
Scan Mode					
TEST	5	7	C6	Id	Scan Mode Test. Only to be used by a Synaptics Test Engineer. Must connect a 100kΩ pull-down to system Ground (GND).
I ² C Slave Interface					
I2C_DEV_ID0	4	5	D8	Id	I²C Device Address Selection (AS): • Default I²C device address is 3B. • Second I²C address 35 is optional by pulling I2C_DEV_ID0 high.
I2C_DEV_ID1	-	6	C7	Id	I²C Device AS (Second Option). Allows two additional I ² C device address options (only available on the CX20811 device).
S_SCL	9	11	F7	Id	I²C Clock.
S_SDA	10	12	F8	Digital I/O	I²C Data.
I ² S/PCM Interface					
MCLK	8	10	G8	Id	System Master Clock. Clock input from the external application host.
RX_CLK	-	14	H7	Digital I/O	I²S/PCM Receive (Rx) Clock (DAC Playback). Master/slave configurable using the control interface.
RX_DATA	-	15	G7	Id	I²S/PCM Rx Data (DAC Playback). Master/slave configurable using the control interface.

Pin Label	Pin Number			I/O Type	Signal Name/Description
	CX20810-11Z	CX20811-11Z	CX20811-15Z		
RX_LRCK	-	16	F6	Digital I/O	I²S/PCM Rx Frame Clock (DAC Playback). Master/slave configurable using the control interface.
TX_CLK	15	17	H6	Digital I/O	I²S/PCM Transmit (Tx) Clock (ADC Record). Master/slave configurable using the control interface.
TX_DATA_1	16	18	E6	Digital Out	I²S/PCM Tx Data 1 (ADC Record). Master/slave configurable using the control interface.
TX_DATA_2	17	19	E5	Digital Out	I²S/PCM Tx Data 2 (ADC Record). Master/slave configurable using the control interface.
TX_LRCK	18	20	G6	Digital I/O	I²S/PCM Tx Frame Clock (ADC Record). Master/slave configurable using the control interface.
Playback Audio Interface					
PVSSN_PWM	-	22	-	GND	PWM GND. GND for the negative side of the PWM H-bridge.
PWM_OUTN	-	23	G5	Oa	PWM Negative Output. Output of the negative side of the PWM H-bridge.
PVDD33_PWM	-	24	F4	PWR	PWM Power. Power to the PWM driver—3V to 3.6V system supply.
PWM_OUTP	-	25	G4	Oa	PWM Positive Output. Output of the positive side of the PWM H-bridge.
PVSSP_PWM	-	26	-	GND	PWM GND. GND for the positive side of the PWM H-bridge.
PVSS_PWM	-	-	G3	GND	PWM GND. GND for the negative and positive side of PWM H-bridge.
Control Signals					
RSTN	19	21	D6	Id	Chip Reset. Active low input pin—internal pull-up. Internally, reset is combined with a Power-On Reset (POR) signal on the VDD pin to ensure the core voltage is stable and high enough before the digital section's reset is released.
Analog VC					
MICBIAS1	21	29	H2	Oa	ADC1 Micbias. Micbias output for channel 1.
ANA_INP1	22	30	G2	Ia	ADC1 Positive Input. Positive microphone input signal for channel 1.
ANA_INN1 ¹	23	31	F2	Ia	ADC1 Negative Input. Negative/GND-sense microphone input signal for channel 1.
MICBIAS2	24	32	F1	Oa	ADC2 Micbias. Micbias output for channel 2.

Pin Label	Pin Number			I/O Type	Signal Name/Description
	CX20810-11Z	CX20811-11Z	CX20811-15Z		
ANA_INP2	25	33	H1	Ia	ADC2 Positive Input. Positive microphone input signal for channel 2.
ANA_INN2 ¹	26	34	G1	Ia	ADC2 Negative Input. Negative/GND-sense microphone input signal for channel 2.
MICBIAS3	34	43	C2	Oa	ADC3 Micbias. Micbias output for channel 3.
ANA_INP3	35	44	A1	Ia	ADC3 Positive Input. Positive microphone input signal for channel 3.
ANA_INN3 ¹	36	45	B1	Ia	ADC3 Negative Input. Negative/GND-sense microphone input signal for channel 3.
MICBIAS4	37	46	B2	Oa	ADC4 Micbias. Micbias output for channel 4.
ANA_INP4	38	47	B3	Ia	ADC4 Positive Input. Positive microphone input signal for channel 4.
ANA_INN4 ¹	39	48	A2	Ia	ADC4 Negative Input. Negative/GND-sense microphone input signal for channel 4.
References					
VDD33_REF	29	37	E1	PWR	3.3V Analog Reference Supply. Source by the analog LDO (VDD_LDO33OUT).
VREF	30	38	D2	Analog I/O	Analog Voltage Reference (VREF). Analog LDO and micbias VREF.
VREFP	31	40	D3	Analog I/O	ADC Positive VREF. Converter high-side sampling reference.
VREFN ¹	32	41	D4	Analog I/O	ADC Negative VREF. Converter low-side sampling reference (0V).
VSS_REF ¹	33	42	C1	GND	Analog Reference GND. GND reference for the VREF generator and analog LDO.
VSS_ANA_3	-	39	D1	GND	Analog GND. GND for the VREF, MICBIAS, and bias current generators.
VSS	-	-	C4, D5	GND	Analog GND/CP GND. Analog GND for CP core, CP switching power stage GND, digital LDO, PLL LDO, and PLLs.
CP					
VDD_CP12OUT	41	51	B4	PWR	CP Output Supply. 1.2V output—use a 10µF load capacitor.
CP12_FLYN	42	52	A4	Analog I/O	CP Fly Capacitor Negative Terminal. Connect to the CP12_FLYP pin through a 1µF capacitor.
VSS_CP12	-	53	-	GND	CP GND. CP switching power stage GND.

Pin Label	Pin Number			I/O Type	Signal Name/Description
	CX20810-11Z	CX20811-11Z	CX20811-15Z		
CP12_FLYP	43	54	B5	Analog I/O	CP Fly Capacitor Positive Terminal. Connect to the CP12_FLYN pin through a 1µF capacitor.
CP12_EN	44	55	C5	Ia	CP Enable Pin: 0V = Disable 3V to 5.5V = Enable
VDD_CP12IN	45	56	-	PWR	CP Input Supply. 3V to 5.5V input voltage for the power stage.
Digital LDO					
LDO33DIG_EN ³	-	57	-	Ia	Digital LDO Enable Pin: 0V = Disable 3V to 5.5V = Enable
LDO33DIG_IN	-	-	A5	Ia	Digital LDO Input Pin and CP Input Supply. Combination of LDO33DIG_EN and VDD_CP12IN.
LDO33DIG_OUT ²	46	58	A6	PWR	Digital LDO Output Supply. 3.3V output.
AVSS_PWR	-	59	-	GND	Analog GND. Analog GND for CP core, digital LDO, PLL LDO, and PLLs.
PLL LDO					
VDD18_PLL	47	60	B6	PWR	Audio Coder-Decoder (CODEC) PLL Supply. 1.8V output.
Analog LDO					
VDD_LDO33IN	27	35	E3	PWR	Analog LDO Input Supply. 3V to 5.5V input, and the supply input for VREF and micbias generators.
VDD_LDO33OUT	28	36	E2	PWR	Analog LDO Output Supply. Nominally 3.4V with 5V input, or 3.14V with 3.3V input. The output tracks the input supply to maintain a selectable minimum headroom of 5% or 10%.
Input Power Pins					
VDD	6	8	D7	PWR	Digital Core Input Power Pin. 1.2V input—connect to VDD_CP12OUT.
VDD33_DIG ⁴	7	9	E7	PWR	Digital I/O Input Power Pin. Connect to the system 3.3V or 1.8V supply.
VDD_I2S ⁴	11	13	H8	PWR	Digital I²S Interface Input Power Pin. Connect to the system 3.3V or 1.8V supply.
VDD33_ANA_1	20	27	F3	PWR	Microphone 1 and 2 Paths Analog Supply Pin. Connect to the analog LDO (VDD_LDO33OUT).
VSS_ANA_1 ¹	-	28	E4	GND	Microphone 1 and 2 Paths GND. Analog GND to the ADC1 and ADC2 paths.

Pin Label	Pin Number			I/O Type	Signal Name/Description
	CX20810-11Z	CX20811-11Z	CX20811-15Z		
VDD33_ANA_2	40	50	A3	PWR	Microphone 3 and 4 Paths Analog Supply Pin. Connect to the analog LDO (VDD_LDO33OUT).
VSS_ANA_2 ¹	-	49	C3	GND	Microphone 3 and 4 Paths GND. Analog GND to the ADC3 and ADC4 paths.

1 = Further grounding information:

- AGND is an isolated, low noise audio GND plane that is only connected to the GND system at the CODEC. All audio traces and components should be placed over this plane.
- MGND is an audio signal GND reference net that needs to connect to VSS_REF at the CODEC (all MGND traces start at VSS_REF). This net is used primarily for SE audio inputs. This net must also connect to the GND system at the CODEC.
- All CODEC audio inputs are differential, and the differential negative input should connect to the signal GND as close as possible to the audio source (typically audio input jack) for SE inputs.

2 = LDO33DIG_OUT:

- Digital LDO input is from VDD_CP12IN, which is 3V to 5.5V.
- For 3.3V systems only—LDO33DIG_OUT may be optionally tied to VDD_CP12IN (bypassing the LDO).
- For CX20811-11Z (QFN 60-pin package) only—if the internal 3.3V digital LDO is disabled, the external 3.3V must be supplied to LDO33DIG_OUT.
- For CX20810-11Z (QFN 48-pin package) and CX20811-15Z (CSP 58-pin package) only—internal 3.3V digital LDO cannot be disabled.

3 = LDO33DIG_EN (60-pin package only):

- Tie to either VDD_CP12IN to enable the internal digital LDO, or GND to disable the internal digital LDO.
- For 3.3V systems only—LDO33DIG_OUT may be optionally tied to VDD_CP12IN (bypassing the LDO).

4 = VDD33_DIG/VDD_I2S:

- VDD33_DIG and VDD_I2S set the digital I/O interface level, and can be tied to 1.8V or 3.3V.
- For the 3.3V interface, tie to the 3.3V rail. Optional—tie to LDO33DIG_OUT if the 3.3V rail is not available.
- For 1.8V interface, tie to the 1.8V rail.

Electrical Characteristics

Absolute Maximum Ratings

The following table lists the devices' absolute maximum ratings.

Table 2: Absolute Maximum Ratings

Parameter	Minimum	Typical	Maximum	Unit	Comments
5V System Voltage Supply					
VDD_CP12IN	−0.4	5	5.5	V	Powers the CP and PLL LDO.
VDD_LDO33IN	−0.4	3.3/5.0	5.5	-	Powers the analog LDO.
3.3V System Voltage Supply					
PVDD33_PWM	−0.4	3.3	3.6	V	Powers the PWM driver.
Digital I/Os					
VDD33_DIG (1.8/3.3)	−0.4	1.8/3.3	3.6	V	Powers the digital I/Os.
VDD_I2S (1.8/3.3)	−0.4	1.8/3.3	3.6	V	Powers the I ² S Interface.
Operating Temperature	−40	-	85	°C	-
Junction Temperature	−40	-	125	°C	-
Storage Temperature	−40	-	150	°C	-

Recommended Operating Conditions

The following table lists the operating conditions that Synaptics recommends for the devices.

Table 3: Recommended Operating Conditions

Parameter	Minimum	Typical	Maximum	Unit	Comments
5V System Voltage Supply					
VDD_CP12IN	3.15	5	5.25	V	Powers the CP and PLL LDO.
VDD_LDO33IN	3.15	3.3/5.0	5.25		Powers the analog LDO.
3.3V System Voltage Supply					
PVDD33_PWM	3.15	3.3	3.45	V	Powers the PWM driver
Digital I/Os @ 1.8V					
VDD33_DIG	1.71	1.8	1.89	V	Powers the 1.8V digital I/Os.
VDD_I2S	1.71	1.8	1.89	V	Powers the 1.8V I ² S Interface.
Digital I/Os @ 3.3V					
VDD33_DIG	3.15	3.3	3.45	V	Powers the 3.3V digital I/Os.
VDD_I2S	3.15	3.3	3.45	V	Powers the 3.3V I ² S Interface.

Device Performance

Depending on the application, the devices can be configured in the following two main functional modes:

- High performance mode = High ADC dynamic range
- Low-power mode = Lower power consumption

There are two high performance modes depending on the enabling of the adaptive biasing of the ADC with the control register. When the adaptive biasing of the ADC is enabled, the ADC power consumption varies dynamically with the amplitude of the ADC input signal. The magnitude of the adaptive bias decreases with the reduced amplitude of the ADC input signal. The ADC in the adaptive biasing mode consumes less power on the average than in the fixed biasing mode when the amplitude of the input signal varies over time. The ADC high performance mode in the adaptive ADC biasing provides the same dynamic range and distortion performance as in the default fixed biasing.

The ADC:

- Low-power mode provides a 3dB lower dynamic range than the high performance mode. The adaptive biasing does not apply to the micbias and PWM.
- High performance and low-power modes can be selected by the control bits in the following table.

Table 4: ADC Performance Mode Register Descriptions

Mode	ADC Biasing	Control Register Address	Control Register Value	Comments
ADC High Performance	ADC Fixed Biasing	0xAD	0x00	Analog ADC clock runs at 12.288MHz.
		0xB3	0x00	
	ADC Adaptive Biasing	0xAD	0x03	
		0xB3	0x04	
ADC Low-power	ADC Adaptive Biasing	0x10	0x7F	Analog ADC clock runs at 6.144MHz.
		0xA5	0x05	
		0xAC	0x30	
		0xAD	0x83	
		0xB3	0x04	
		0xB4	0xA0	
		0xBA	0x06	

The following table shows the devices' performance in both high performance modes, with and without enabling the adaptive ADC biasing.

Table 5: Device Performance in High Performance Mode

Parameter	Minimum	Typical	Maximum	Unit	Comments
Microphone Input					
Dynamic Range (A-weighted)					• 997Hz • Measured using a –60dBFS reference signal • A-weight filtering
Programmable Gain Amplifier (PGA) = 0dB	-	106	-	dBA	
PGA = 6dB	-	106	-		
PGA = 12dB	-	105	-		
PGA = 24dB	-	100	-		
PGA = 30dB	-	95	-		

Table 5: Device Performance in High Performance Mode (Continued)

Parameter	Minimum	Typical	Maximum	Unit	Comments	
THD+N					997Hz tone	
PGA = 0dB	-	−89	-	dBc	- The amount of distortion and noise with an audio band relative to the test signal - Tested at −1dBFS	
PGA = 6dB	-	−85	-			
PGA = 12dB	-	−85	-			
PGA = 24dB	-	−84	-			
PGA = 30dB	-	−84	-			
Power Supply Rejection Ratio (PSRR)	-	90	-	dB	At 1kHz.	
Crosstalk	-	90	-	dB	-	
Input Resistance					For gains = 3dB–30dB, input resistance is programmable:	
PGA = −6dB	-	16	-	kΩ	500kΩ (default)	
PGA= 0dB	-	8	-		250kΩ	
PGA = 3dB–30dB	-	500	-		125kΩ	
					25kΩ	
Micbias						
Bias Voltage	1.5	-	4	V	-	
Bias Current	-	-	10	mA	-	
Noise in the Signal Band Width (BW)	-	−116	-	dBV	20Hz–20kHz.	
PWM (CX20811 Only)						
Full-scale Output	-	2	-	V _{RMS}	Scales with the PWM supply.	
SNR (A-weighted)	-	88.8	-	dBA	- Measured using a −60dBFS reference signal - Use an A-weight filter - Tested with a 4Ω load	
THD+N					dBc	The amount of distortion and noise relative to the test signal. Tested with a 4Ω load.
0dBFS	-	−39.9	-			
−1dBFS	-	−49.1	-			
−3dBFS	-	−53.1	-			
−10dBFS	-	−64.3	-			

Note:

- Test conditions, unless otherwise noted:
 - $T_A = 27^\circ\text{C}$
 - Input supply = 3.3V
 - $F_s = 48\text{kHz}$
 - MCLK = 12.288MHz (an internal PLL is not used) or 24.000MHz (with an internal PLL)
- Performance was measured using the EVK, which uses 0.01μF capacitors in series with input negative and positive pins. See "Mic-In PGA" on page 82 for additional details of the input configurations.

The following table shows the devices' performance in low-power mode. The performance of the micbias and PWM does not change in low-power mode.

Table 6: Device Performance in Low-Power Mode

Parameter	Minimum	Typical	Maximum	Unit	Comments
Microphone Input					
Dynamic Range (A-weighted)					997Hz
PGA = 0dB	-	103	-	dBA	Measured using a -60dBFS reference signal
PGA = 6dB	-	103	-		A-weight filtering
THD+N					997Hz tone
PGA = 0dB	-	-88	-	dBc	The amount of distortion and noise with an audio band that is relative to the test signal
PGA = 6dB	-	-85	-		Tested at -1dBFS

Note:

- Test conditions, unless otherwise noted:
 - $T_A = 27^{\circ}\text{C}$
 - Input supply = 3.3V
 - $F_s = 48\text{kHz}$
 - MCLK = 12.288MHz (an internal PLL is not used) or 24.000MHz (with an internal PLL)
- Performance was measured using the EVK, which uses 0.01 μF capacitors in series with input negative and positive pins. See "Mic-In PGA" on page 82 for additional details of the input configurations.

Power Consumption

The following table shows the devices' power consumption in the high performance modes and low-power mode.

Table 7: Device Power Consumption in High Performance Mode (ADC Fixed Biasing)

Device State	CP	VREF	Analog LDO	Digital LDO	PLL LDO	PLL	Current from System 3.3V (mA)
Sleep	Disabled (Pin)	Disabled	Disabled	Bypassed	Disabled	Disabled	0.009
Standby Analog Off	Enabled (Pin)	Disabled	Disabled	Bypassed	Disabled	Disabled	0.66
Standby Analog On	Enabled (Pin)	Enabled	Enabled	Bypassed	Disabled	Disabled	1.25
One ADC in High Performance Mode with –1dBFS Input, 997Hz	Enabled (Pin)	Enabled	Enabled	Bypassed	Enabled	Enabled (24MHz)	10.61
Two ADCs in High Performance Mode with –1dBFS Input, 997Hz	Enabled (Pin)	Enabled	Enabled	Bypassed	Enabled	Enabled (24MHz)	17.85
Four ADCs in High Performance Mode with –1dBFS Input, 997Hz	Enabled (Pin)	Enabled	Enabled	Bypassed	Enabled	Enabled (24MHz)	33.84
DAC with –60dBFS, 40μW Output (CX20811 Only)	Enabled (Pin)	Disabled	Disabled	Bypassed	Disabled	Disabled	5.88
DAC with –10dBFS, 97mW Output (CX20811 Only)	Enabled (Pin)	Disabled	Disabled	Bypassed	Disabled	Disabled	37.6
DAC with 0dBFS, 970mW Output (CX20811 Only)	Enabled (Pin)	Disabled	Disabled	Bypassed	Disabled	Disabled	333

Note:

- The CP is enabled by a pull-up at the pin.
- The digital LDO (pin) is disabled and bypassed by connecting its input to the output.
- The PLL LDO is enabled/disabled by a register change.
- For DAC, the system current listed includes the power that is delivered to the load.
- For DAC, the MCLK frequency used is 12.288MHz—the PLL was not used or needed.
- The load on the PWM output is 4Ω + 22μH.

Table 8: Device Power Consumption in High Performance Mode (ADC Adaptive Biasing)

Device State	CP	VREF	Analog LDO	Digital LDO	PLL LDO	PLL	Current from System 3.3V (mA)
One ADC in High Performance Mode with –1dBFS Input, 997Hz	Enabled (Pin)	Enabled	Enabled	Bypassed	Enabled	Enabled (24MHz)	10.22
One ADC in High Performance Mode with –60dBFS Input, 997Hz	Enabled (Pin)	Enabled	Enabled	Bypassed	Enabled	Enabled (24MHz)	6.69

Table 9: Device Power Consumption in Low-Power Mode

Device State	CP	VREF	Analog LDO	Digital LDO	PLL LDO	PLL	Current from System 3.3V (mA)
One ADC in Low Power Mode with –1dBFS Input, 997Hz	Enabled (Pin)	Enabled	Enabled	Bypassed	Enabled	Enabled (24MHz)	7.12
One ADC in Low Power Mode with –60dBFS Input, 997Hz	Enabled (Pin)	Enabled	Enabled	Bypassed	Enabled	Enabled (24MHz)	4.49

Device Description

Device Power Management and Power Up Sequence

When VDD_CORE is supplied to CX20810/CX20811 devices, then there are no specific sequencing requirements.

- If VDD_CORE is not applied (for example to conserve power), and power is applied to VDD_DIG and VDD_I2S, then it is required that VDD_CORE be enabled momentarily.
- If the VDD_DIG and VDD_I2S supplies are disconnected and reconnected, then VDD_CORE must be power cycled on again, even if only momentarily.

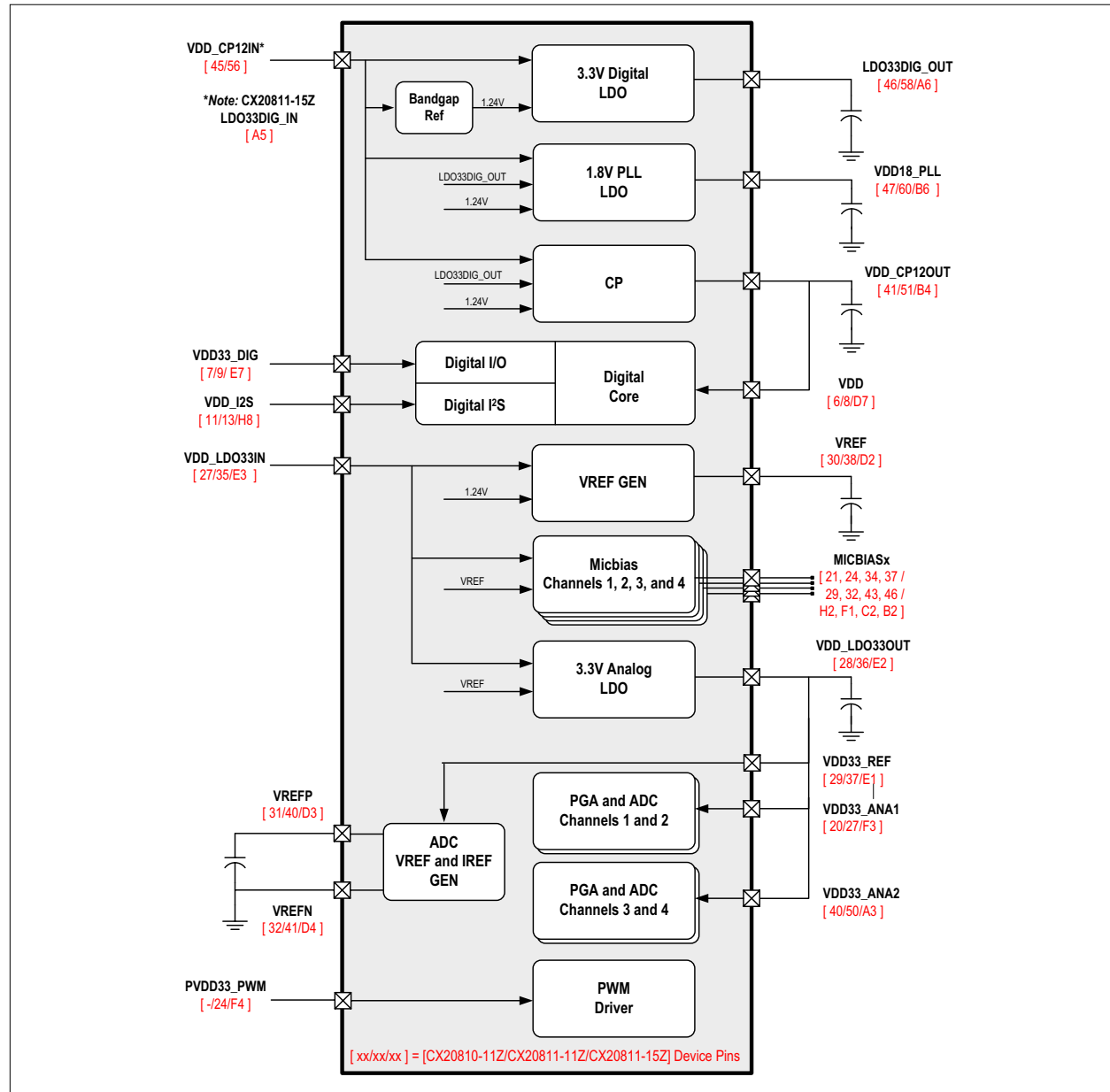


Figure 7: Device Power Management

Digital Low Dropout (LDO)

Block Diagram

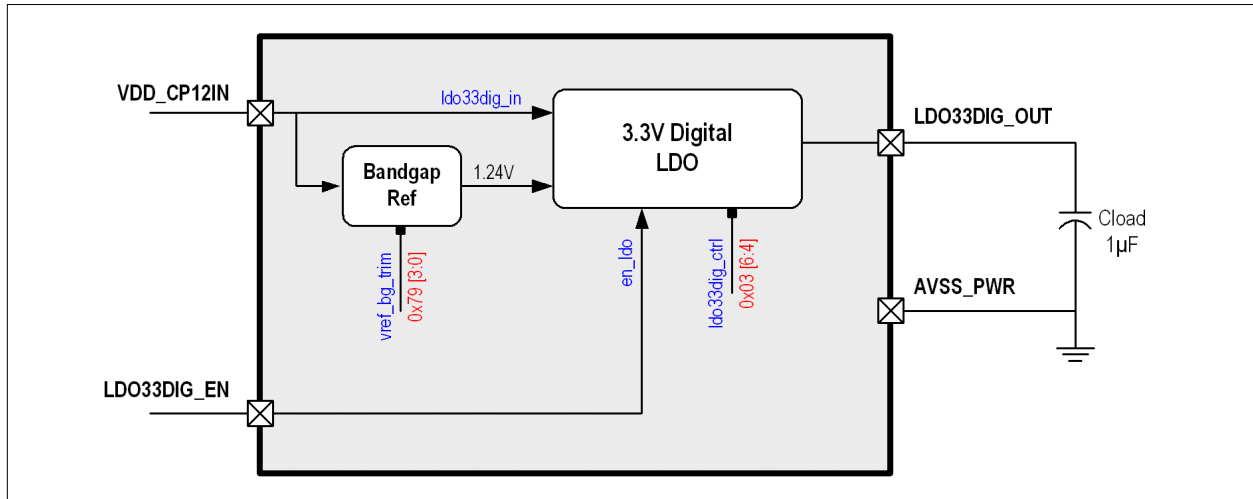


Figure 8: CX20810/CX20811-11Z Digital LDO Block Diagram

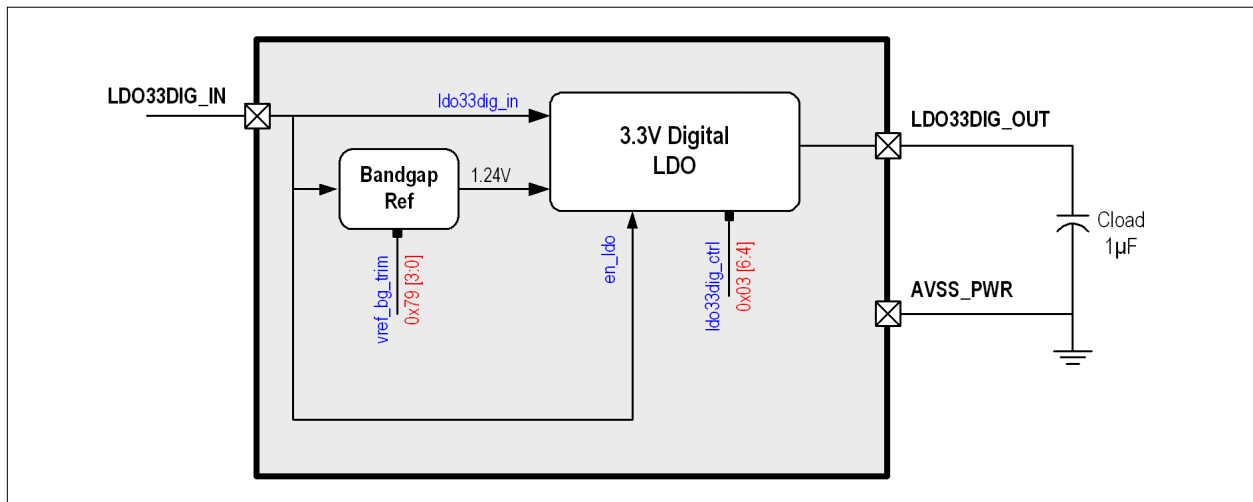


Figure 9: CX20811-15Z Digital LDO Block Diagram

Block Description

The digital LDO provides a 3.3V digital supply for the CP and PLL LDO, as well as a digital supply for logic cells in all other LDOs. A 50mA current limit is also implemented within the cell. In systems where the incoming supply is greater than 3.6V, this LDO can be used to provide 3.3V to the device. If the system supply is limited to 3.3V, then this LDO can be disabled and the incoming 3.3V supply should be connected to VDD_CP12IN (LDO33DIG_IN on the CX20811-15Z) and LDO33DIG_OUT.

Note: The VDD_CP12IN (LDO33DIG_IN on the CX20811-15Z) pin must be connected to a supply rail in all configurations to provide power to the bandgap reference.

Pin Description

For definitions of the I/O Type acronyms used in the following table, see ["Signal Definitions"](#) on page 34.

Table 10: Digital LDO Pin Description

Pin Label	Pin Number			I/O Type	Signal Name/Description
	CX20810-11Z	CX20811-11Z	CX20811-15Z		
LDO33DIG_EN ¹	-	57	-	Ia	Digital LDO Enable Pin: 0V = Disable 1.8V to 5.5V = Enable
LDO33DIG_IN	-	-	A5	Ia	Digital LDO Input Pin and CP Input Supply. Combination of LDO33DIG_EN and VDD_CP12IN.
LDO33DIG_OUT	46	58	A6	PWR	Digital LDO Output Supply. 3.3V output.
VDD_CP12IN	45	56	-	PWR	CP Input Supply. 3V to 5.5V input voltage—also bonded to LDO33DIG_IN.
AVSS_PWR	-	59	-	GND	Analog GND. Analog GND for the CP core, digital LDO, PLL LDO, and PLLs.
VSS	-	-	C4, D5	GND	Analog GND/CP GND. Analog GND for the CP core, CP switching power stage GND, digital LDO, PLL LDO, and PLLs.

¹ = In the CX20810 device, LDO33DIG_EN is bonded to VDD_CP12IN.

Register Description

Table 11: REF_CTRL_2—0x79

Bits	Name	Default	R/W	Description
3:0	VREF_BG_TRIM [3:0]	0	R/W	Bandgap VREF trimming: • 0 = 1.238V • 1 = 1.232V • 2 = 1.225V • 3 = 1.219V • 4 = 1.212V • 5 = 1.205V • 6 = 1.198V • 7 = 1.192V • 8 = 1.292V • 9 = 1.286V • 10 = 1.279V • 11 = 1.272V • 12 = 1.265V • 13 = 1.258V • 14 = 1.252V • 15 = 1.245V

Table 12: PWR_CTRL_3—0x03

Bits	Name	Default	R/W	Description
7	LDO33DIG_DIS_ILIM	0	R/W	Disable output current limiting for the digital LDO: • 0 = Enables the 50mA current limit • 1 = Current limit disabled
6:4	LDO33DIG_CTRL [2:0]	0	R/W	Control digital LDO output voltage: • 0 = 3.31V • 1 = 3.25V • 2 = 3.19V • 3 = 3.13V • 4 = 3.55V • 5 = 3.49V • 6 = 3.43V • 7 = 3.37V

Performance Data

Table 13: Digital LDO Specifications

Parameter	Minimum	Typical	Maximum	Unit
Temperature	–40	27	125	°C
Supply Voltage—VDD5	3	5	5.5	V
Output Voltage	–	3.3	–	V
Clload	0.8	1	12	μF
Equivalent Series Resistance (ESR)	–	–	500	mΩ
Load Current	0	–	50	mA
Current Limit Threshold	50	–	–	mA

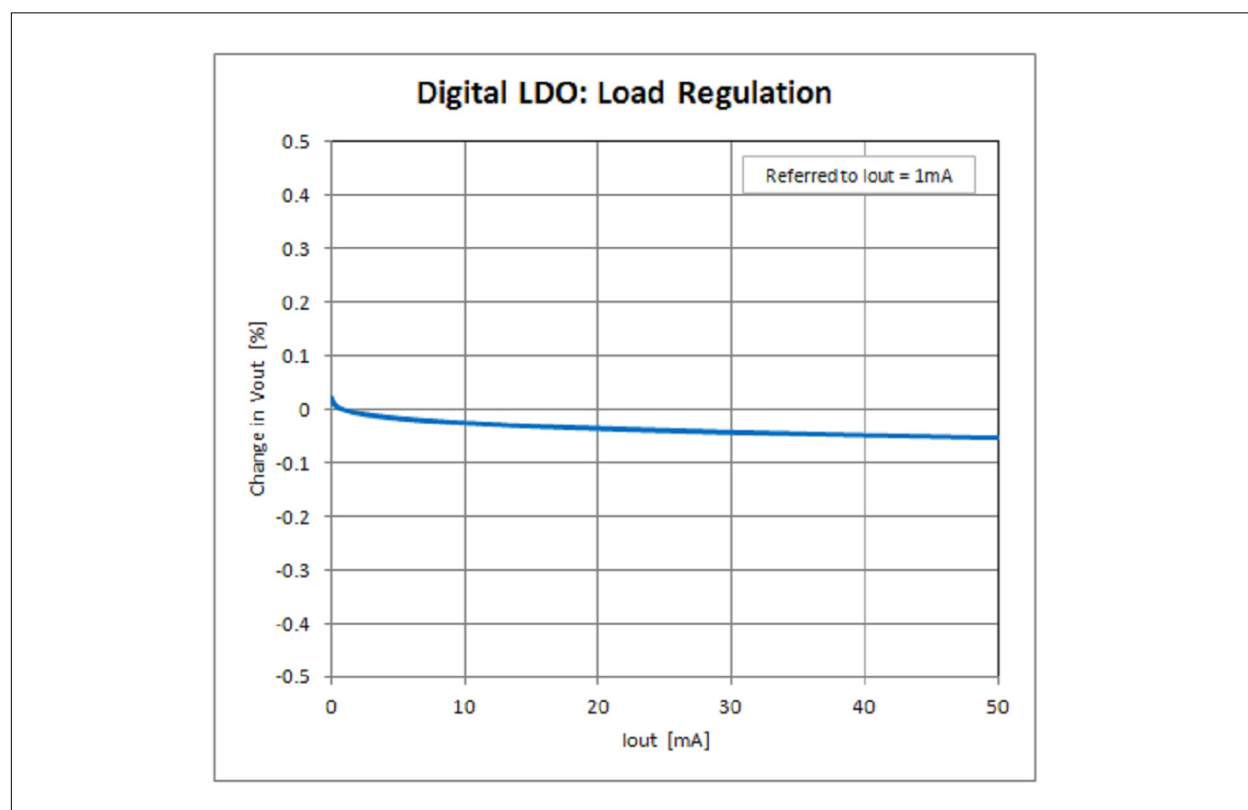


Figure 10: Digital LDO Load Regulation

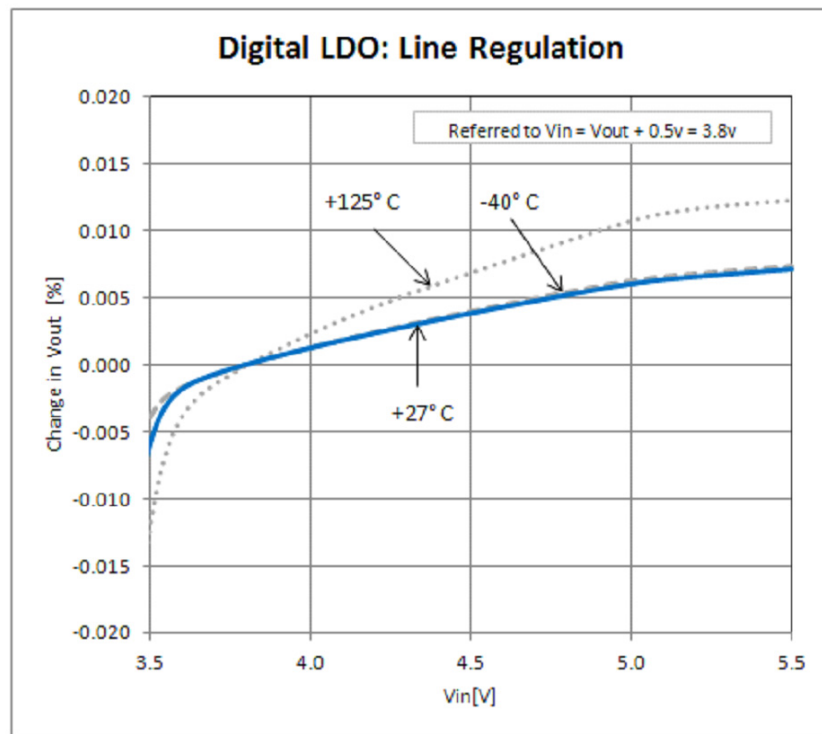


Figure 11: Digital LDO Line Regulation

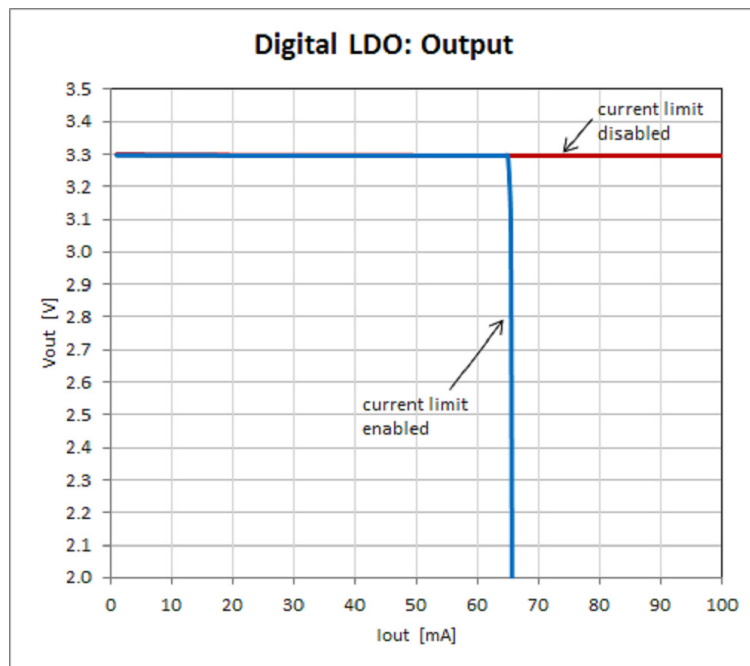


Figure 12: Digital LDO Current Limiting

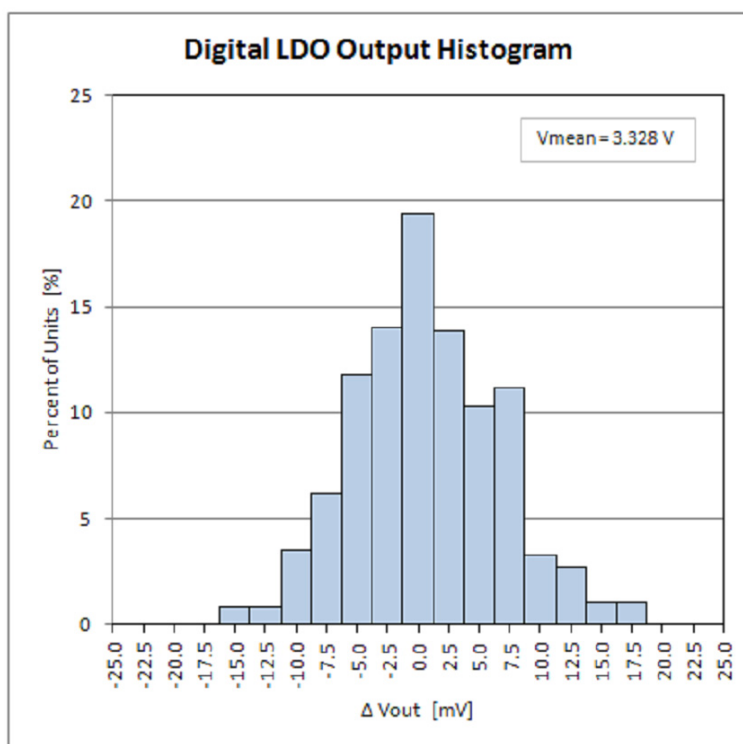


Figure 13: Digital LDO Output Histogram

Phase Locked Loop (PLL) LDO

Block Diagram

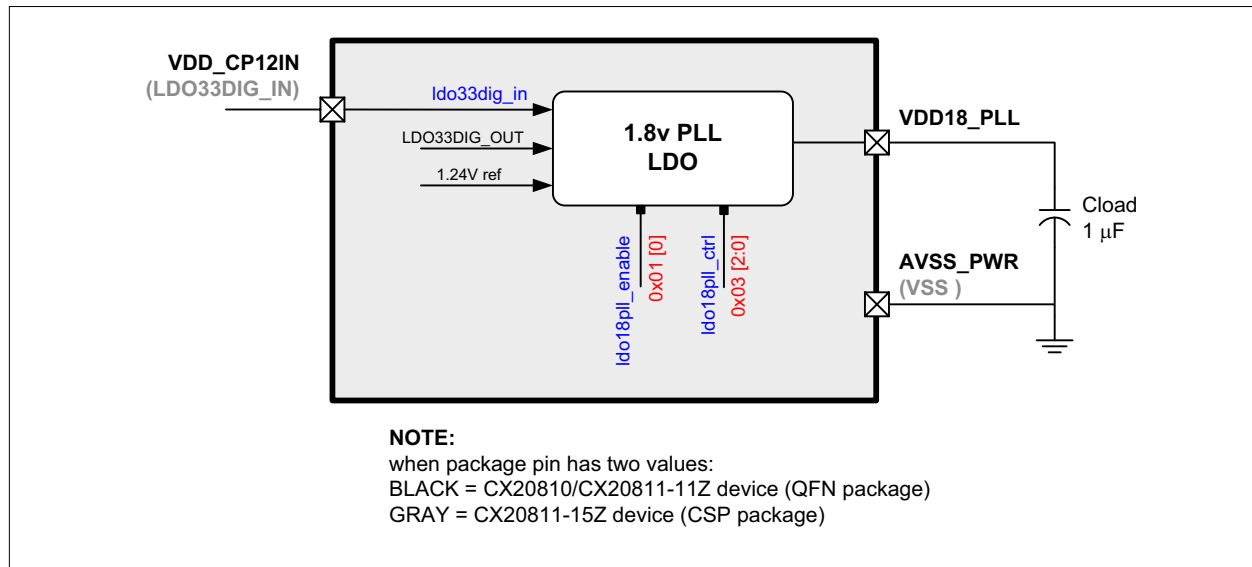


Figure 14: CX20810/CX20811-11Z PLL and CX20811-15Z PLL LDO Block Diagrams

Block Description

The PLL LDO provides a 1.8V digital supply for the integrated PLL. If an external system 1.8V supply is available, then this LDO can be disabled and the external supply can be connected directly to the VDD18_PLL pin—also enable 0x04 [0] (pll_force_por18) to bypass the LDO gating on the PLL clock.

The operation of this block is similar to the 3.3V digital LDO, except that the cell enable is only register controlled (0x01 [0]).

Note: The VDD_CP12IN (LDO33DIG_IN on the CX20811-15Z) pin must be connected to a supply rail in all configurations to provide power to the bandgap reference.

Pin Description

For definitions of the I/O Type acronyms used in the following table, see "Signal Definitions" on page 34.

Table 14: PLL LDO Pin Description

Pin Label	Pin Number			I/O Type	Signal Name/Description
	CX20810-11Z	CX20811-11Z	CX20811-15Z		
VDD18_PLL	47	60	B6	PWR	Audio CODEC PLL Supply. 1.8V output.
VDD_CP12IN	45	56	-	PWR	CP Input Supply. 3V to 5.5V input voltage—also bonded to LDO33DIG_IN.
LDO33DIG_IN	-	-	A5	Ia	Digital LDO Input Pin and CP Input Supply. Combination of LDO33DIG_EN and VDD_CP12IN.
AVSS_PWR	-	59	-	GND	Analog GND. Analog GND for the CP core, digital LDO, PLL LDO, and PLLs.
VSS	-	-	C4, D5	GND	Analog GND/CP GND. Analog GND for the CP core, CP switching power stage GND, digital LDO, PLL LDO, and PLLs.

Register Description

Table 15: PWR_CTRL_1—0x01

Bits	Name	Default	R/W	Description
0	LDO18PLL_ENABLE	0	R/W	Enables the 1.8V LDO for the PLL: 0 = LDO disabled 1 = Enables the LDO

Table 16: PWR_CTRL_3—0x03

Bits	Name	Default	R/W	Description
3	LDO18PLL_DIS_ILIM	0	R/W	Disable output current limiting for PLL LDO: 0 = Enables the 50mA current limit 1 = Current limit disabled
2:0	LDO18PLL_CTRL [2:0]	0	R/W	Control 1.8V LDO output voltage: 0 = 1.80V 1 = 1.69V 2 = 1.58V 3 = 1.46V 4 = 2.25V 5 = 2.14V 6 = 2.03V 7 = 1.92V

Performance Data

Table 17: PLL LDO Specifications

Parameter	Minimum	Typical	Maximum	Unit
Temperature	−40	27	125	°C
Supply Voltage—VDD5	3	5	5.5	V
Output Voltage	—	1.8	—	V
Cload	0.8	1	12	μF
ESR	—	—	500	mΩ
Load Current	0	—	50	mA
Current Limit Threshold	50	—	—	mA

Because the same core cells were re-used for the PLL LDO, the performance plots are similar to the digital LDO.

Charge Pump (CP)

Block Diagram

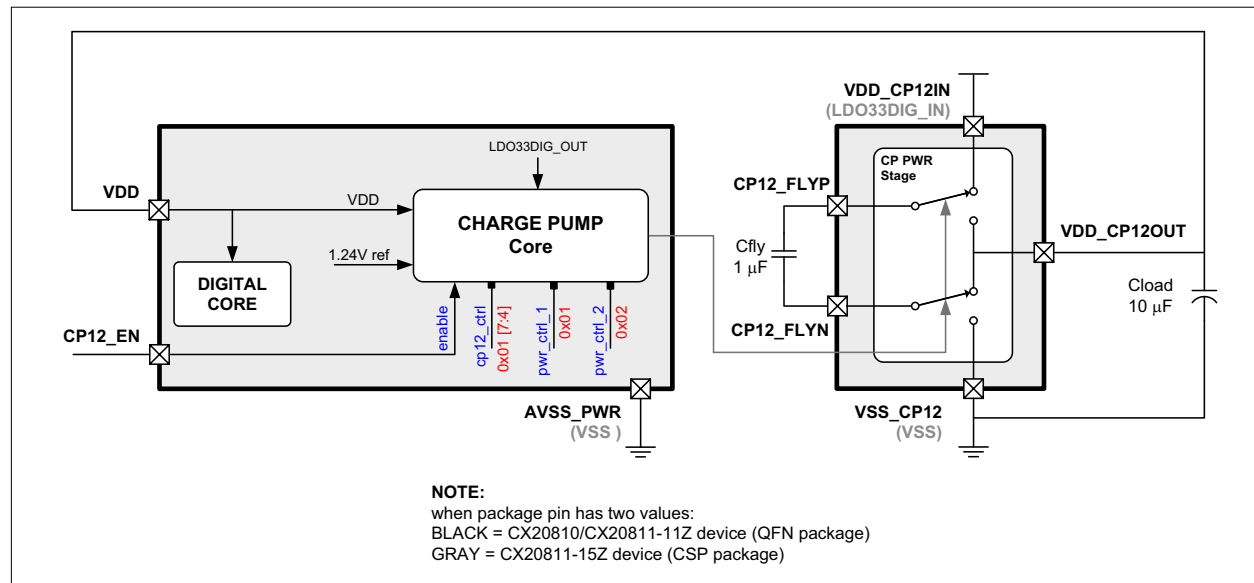


Figure 15: CX20810/CX20811-11Z and CX20811-15Z CP Block Diagram

Block Description

A capacitive divide-by-2 CP is implemented to efficiently convert the incoming system supply voltage to the 1.2V supply level required by the digital core. Compared to a traditional LDO with an efficiency at a large load current of $\epsilon = V_{out}/V_{in}$, the CP's efficiency is $\epsilon = 2 \cdot V_{out}/V_{in}$, or twice as efficient.

Example: In the case of a 5V system supply being converted to 1.2V, the CP efficiency is 48%, compared to 24% for an LDO. Similarly, if the system supply is 3.3V, the CP efficiency is 73% vs 36% for an LDO.

Typically the CP output is tied externally to the digital core pin VDD (CX20810/CX20811-11Z pin 6, CX20811-11Z pin 8, and CX20811-15Z pin D7). When the CP12_EN CP enable pin is high, the digital reset is an AND-ing of the RSTN pin signal, an internal POR circuit on the VDD pin, and the CP state (the CP must be in its full-drive active state as opposed to its weak initial soft-start state). If the CP is to be bypassed and an external 1.2V supply is to be applied, CP12_EN must be held low and a digital reset is then an AND-ing of the RSTN pin and POR on VDD.

Pin Description

For definitions of the I/O Type acronyms used in the following table, see ["Signal Definitions"](#) on page 34.

Table 18: CP Pin Description

Pin Label	Pin Number			I/O Type	Signal Name/Description
	CX20810-11Z	CX20811-11Z	CX20811-15Z		
CP12_EN	44	55	C5	Ia	CP Enable Pin: 0V = Disable 3V to 5.5V = Enable
VDD_CP12IN	45	56	-	PWR	CP Input Supply. 3V to 5.5V input voltage—also bonded to LDO33DIG_IN.
LDO33DIG_IN	-	-	A5	Ia	Digital LDO Input Pin and CP Input Supply. Combination of LDO33DIG_EN and VDD_CP12IN.
VSS_CP12	-	53	-	GND	CP GND. CP switching power stage GND.
VDD_CP12OUT	41	51	B4	PWR	CP Output Supply. 1.2V output—use a 10µF load capacitor.
CP12_FLYP	43	54	B5	Analog I/O	CP Fly Capacitor Positive Terminal. Connect to the CP12_FLYN pin through a 1µF capacitor.
CP12_FLYN	42	52	A4	Analog I/O	CP Fly Capacitor Negative Terminal. Connect to the CP12_FLYP pin through a 1µF capacitor.
AVSS_PWR	-	59	-	GND	Analog GND. Analog GND for the CP core, digital LDO, PLL LDO, and PLLs.
VSS	-	-	C4, D5	GND	Analog GND/CP GND. Analog GND for the CP core, CP switching power stage GND, digital LDO, PLL LDO, and PLLs.

Register Description

Table 19: PWR_CTRL_1—0x01

Bits	Name	Default	R/W	Description
7:4	CP12_CTRL [3:0]	0	R/W	CP output voltage programming: 0 = 1.200V 1 = 1.175V 2 = 1.150V 3 = 1.125V 4 = 1.100V 5 = 1.075V 6 = 1.050V 7 = 1.025V 8 = 1.400V 9 = 1.375V 10 = 1.350V 11 = 1.325V 12 = 1.300V 13 = 1.275V 14 = 1.250V 15 = 1.225V
3	CP12_SENSE_SELECT	0	R/W	CP feedback sensing mux: 0 = vdd_core (normal behavior) 1 = vdd_cp12out (test mode)
2:1	CP12_LOOPMODE [1:0]	0	R/W	CP operation mode control: 0 = Normal (linear plus skip) 1 = Linear only 2 = Skip only (do not use with the 5V supply) 3 = Power stage disabled and put into a high-Z state (test mode only)

Table 20: PWR_CTRL_2—0x02

Bits	Name	Default	R/W	Description
7:6	CP12_SENSE_FILT [1:0]	0	R/W	CP sense filter time constant: 0 = 2ns 1 = 150ns 2 = 300ns 3 = 600ns
5:4	CP12_FILT_SELW [1:0]	0	R/W	CP loop-filter slew rate control: 0 = 51mV/μs 1 = 84mV/μs 2 = 26mV/μs 3 = 32mV/μs
3	CP12_COMP_FF_EN	0	R/W	CP sample and hold of the loop filter input: 0 = No sampling (normal) 1 = Use sampling and hold
2	CP12_FORCE_ENABLE	0	R/W	CP software enable: 0 = Enables the CP using the CP12_EN pin 1 = Force the CP on using the bit
1	CP12_FORCE_RSTB	0	R/W	CP POR detection on the 3.3V: 0 = 3.3V supply on the LDO33DIG pin is monitored—resets and disables the CP if the voltage is below 2.4V 1 = POR is disabled
0	CP12_CLKDET_BYPASS	0	R/W	Bypasses the CP clock detection circuitry: 0 = Enables the clock detection 1 = Clock detection disabled

Performance Data

Table 21: CP Specifications

Parameter	Minimum	Typical	Maximum	Units
Temperature	−40	27	125	°C
Supply Voltage—VDD_CP12IN	3	5	5.50	V
Supply Voltage—LDO33DIG_OUT	2.8	3.3	3.6	V
Oscillator Frequency ¹	430	550	700	kHz
Capacitors				
Cfly	-	1μF	-	-
Cload	-	10μF	-	-
ESR	-	50mΩ	-	-
Load Current	-	-	50	mA
Inrush Current	-	-	100mA (50μC)	-

1 = The maximum output switching rate is half the oscillator frequency since it takes two clock cycles to sample and transfer charge from the input supply to the output load capacitor. The high variance in the oscillator frequency is because the oscillator is a crude internal RC oscillator that is sensitive to process variations. When in light load conditions, the control loop will skip a large number of cycles and the effective output switching rate will be very low (in the 1 Hz range when load current is zero).

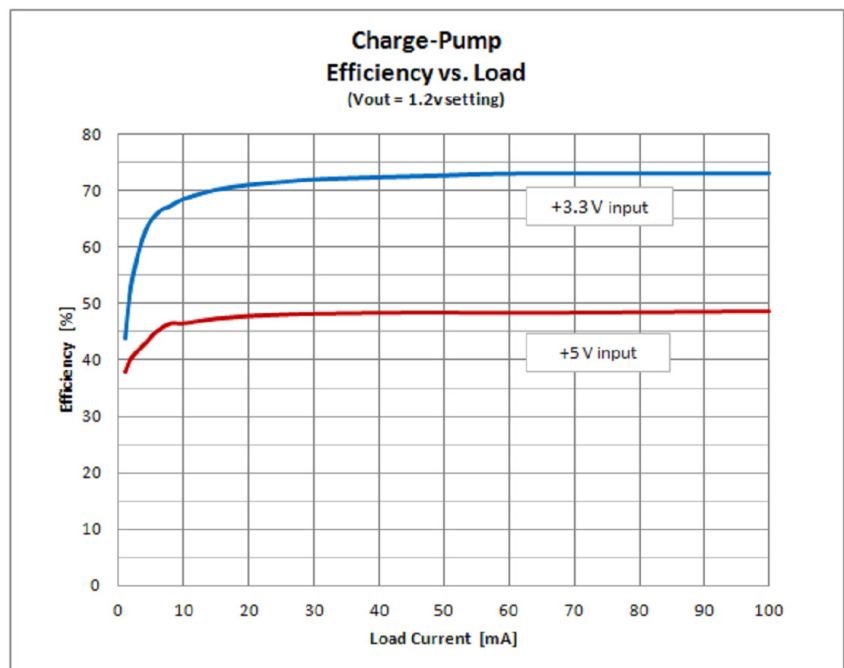


Figure 16: CP Efficiency vs Load Current

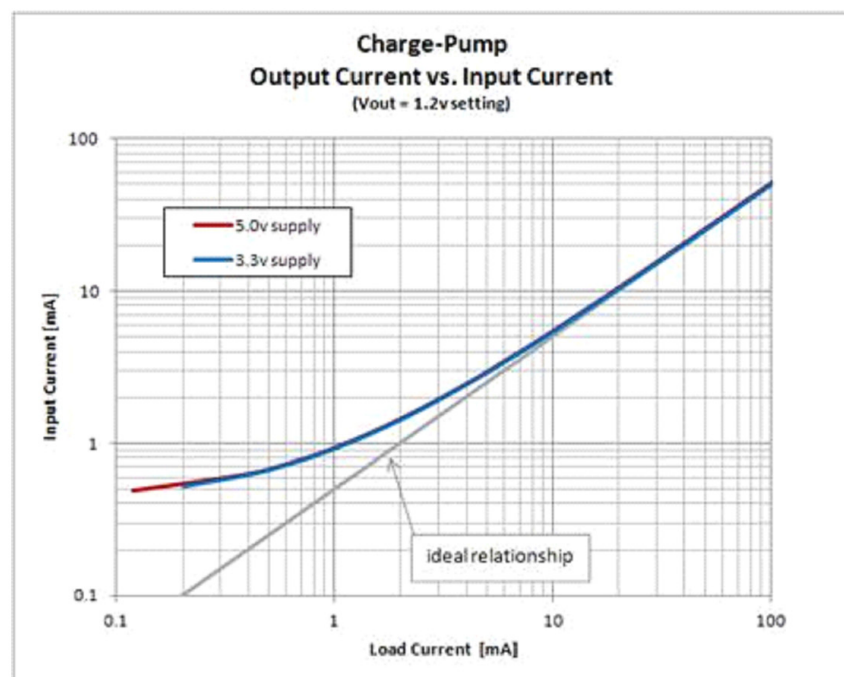


Figure 17: CP Current Transfer

Voltage Reference (VREF) Generator

Block Diagram

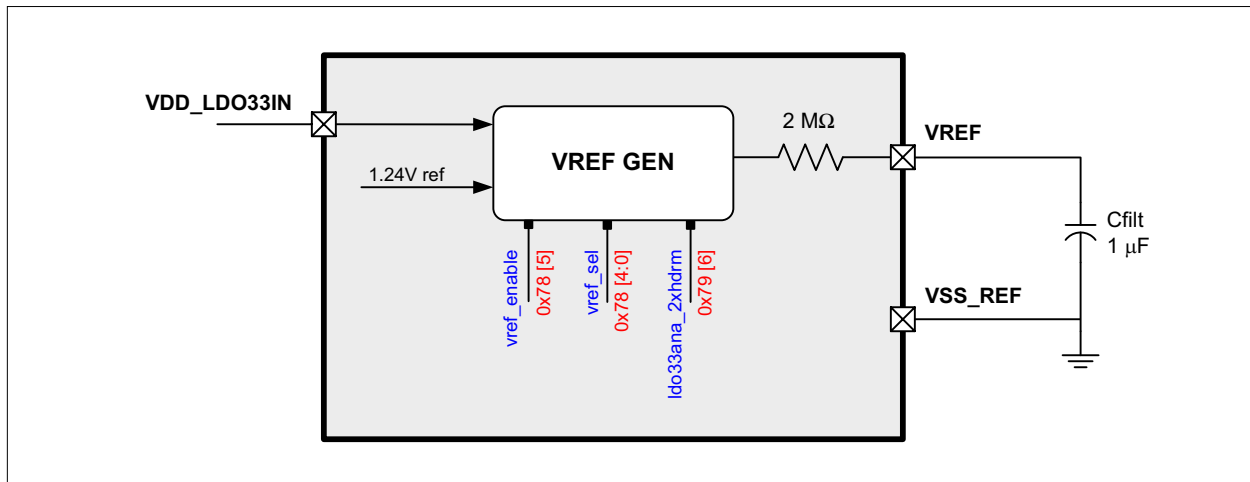


Figure 18: VREF Generator Block Diagram

Block Description

The VREF generator creates a low-noise VREF for the analog LDO and each channel's micbias generator. An internal 2mΩ series resistor is included to create a low frequency Low-Pass Filter (LPF) with an external 1μF filter capacitor.

Because the micbias generators are configured as unity-gain amplifiers to maintain excellent noise performance, programmability of the micbias voltage is achieved in the VREF generator cell. The programming is defined as:

- $VREF = 2.48V * (N + 15 / 25)$, $VDD_LDO33IN > 3.6V$
- $VREF = VDD_LDO33IN * (N + 15 / 36)$, $VDD_LDO33IN < 3.6V$ & $ldo33ana_2xhdrn = 0$
- $VREF = VDD_LDO33IN * (N + 15 / 38)$, $VDD_LDO33IN < 3.6V$ & $ldo33ana_2xhdrn = 1$

...where:

- $N = VREF_SEL = \text{Register } 0x78 [4:0]$
- $LDO33ANA_2XHDRM = \text{Register } 0x79 [6]$

Conversely, for a desired VREF (and micbias) voltage the control code is calculated as:

- $N = 10.1 * VREF - 15$, $VDD_LDO33IN > 3.6 V$
- $N = 36 * (VREF / VDD_LDO33IN) - 15$, $VDD_LDO33IN < 3.6V$ & $ldo33ana_2xhdrn = 0$
- $N = 38 * (VREF / VDD_LDO33IN) - 15$, $VDD_LDO33IN < 3.6V$ & $ldo33ana_2xhdrn = 1$

The supply tracking at lower supply voltages ensures that there is minimum headroom between the input supply and the analog LDO output voltage, and this ensures a high PSRR in the analog LDO. This minimum headroom is programmable to either 5% or 10% through register 0x79 [6].

The VREF generator also includes a “fast-start” circuit that effectively bypasses the series resistor and actively charges up the filter capacitor to ensure a quick initial ramp-up. When the output has reached its final value, the pull-up circuitry automatically disengages and the resistor helps filter the VREF output noise.

Pin Description

For definitions of the I/O Type acronyms used in the following table, see "Signal Definitions" on page 34.

Table 22: VREF Generator Pin Description

Pin Label	Pin Number			I/O Type	Signal Name/Description
	CX20810-11Z	CX20811-11Z	CX20811-15Z		
VDD_LDO33IN	27	35	E3	PWR	Analog LDO Input Supply. 3V to 5.5V input—also the supply input for VREF and micbias generators.
VREF	30	38	D2	Analog I/O	Analog VREF. Analog LDO and micbias VREF.
VSS_REF	33	42	C1	GND	Analog Reference GND. GND reference for the VREF generator and analog LDO.

Register Description

Table 23: REF_CTRL_1—0x78

Bits	Name	Default	R/W	Description
5	VREF_ENABLE	0	R/W	Enables the VREF (needed for the analog LDO and micbias): 0 = Disables the VREF 1 = Enables the VREF
4:0	VREF_SEL	0	R/W	Control VREF output and micbias voltage: - AVDD5 = 5V: - VREF = $1.5 + 0.1 * \text{VREF_SEL}$ (maximum VREF is 4V → maximum vref_sel = 25 decimal) - AVDD5 = 3.3V: - VREF = $\text{AVDD5} * (\text{VREF_SEL} + 15)/36$ if headroom = 5% (0x79 [6] = 0) - VREF = $\text{AVDD5} * (\text{VREF_SEL} + 15)/38$ if headroom = 10% (0x79 [6] = 1) - VREF maximum is always $0.95 * \text{AVDD5}$

Table 24: REF_CTRL_2—0x79

Bits	Name	Default	R/W	Description
6	LDO33ANA_2XHDM	0	R/W	Controls the minimum headroom between the analog LDO input and output. At input supplies near the target output voltage, the output tracks lower to ensure good PSRR: 0 = LDO headroom is 5% 1 = LDO headroom is 10%
4	VREF_FASTSTART_DISABLE	0	R/W	Disables the fast-start circuit on VREF: 0 = Enables fast-start 1 = Disables the fast-start

Performance Data

Table 25: VREF Specifications

Parameter	Minimum	Typical	Maximum	Units
Temperature	−40	27	125	°C
Supply Voltage—VDD_LDO33IN	2.7	3.3/5	5.5	V
Output Voltage	1.5	-	4	V
Load	-	1	-	μF
Output Noise	-	−120	-	dBV

Table 26: VREF vs Code

vref_sel 0x78 [4:0]	VDD_LDO33IN = 5V Headroom 0x79 [6] = x	VDD_LDO33IN = 3.3V	
		Headroom 0x79 [6] = 0	Headroom 0x79 [6] = 1
0	1.50	1.38	1.30
1	1.60	1.47	1.39
2	1.70	1.56	1.48
3	1.80	1.65	1.56
4	1.90	1.74	1.65
5	2.00	1.83	1.74
6	2.10	1.93	1.82
7	2.20	2.02	1.91
8	2.30	2.11	2.00
9	2.40	2.20	2.08
10	2.50	2.29	2.17
11	2.60	2.38	2.26
12	2.70	2.48	2.34
13	2.80	2.57	2.43
14	2.90	2.66	2.52
15	3.00	2.75	2.61
16	3.10	2.84	2.69
17	3.20	2.93	2.78
18	3.30	3.03	2.87
19	3.40	3.12	2.95
20	3.50	3.14	3.04
21	3.60	3.14	3.13
22	3.70	3.14	3.14
23	3.80	3.14	3.14
24	3.90	3.14	3.14
25	4.00	3.14	3.14

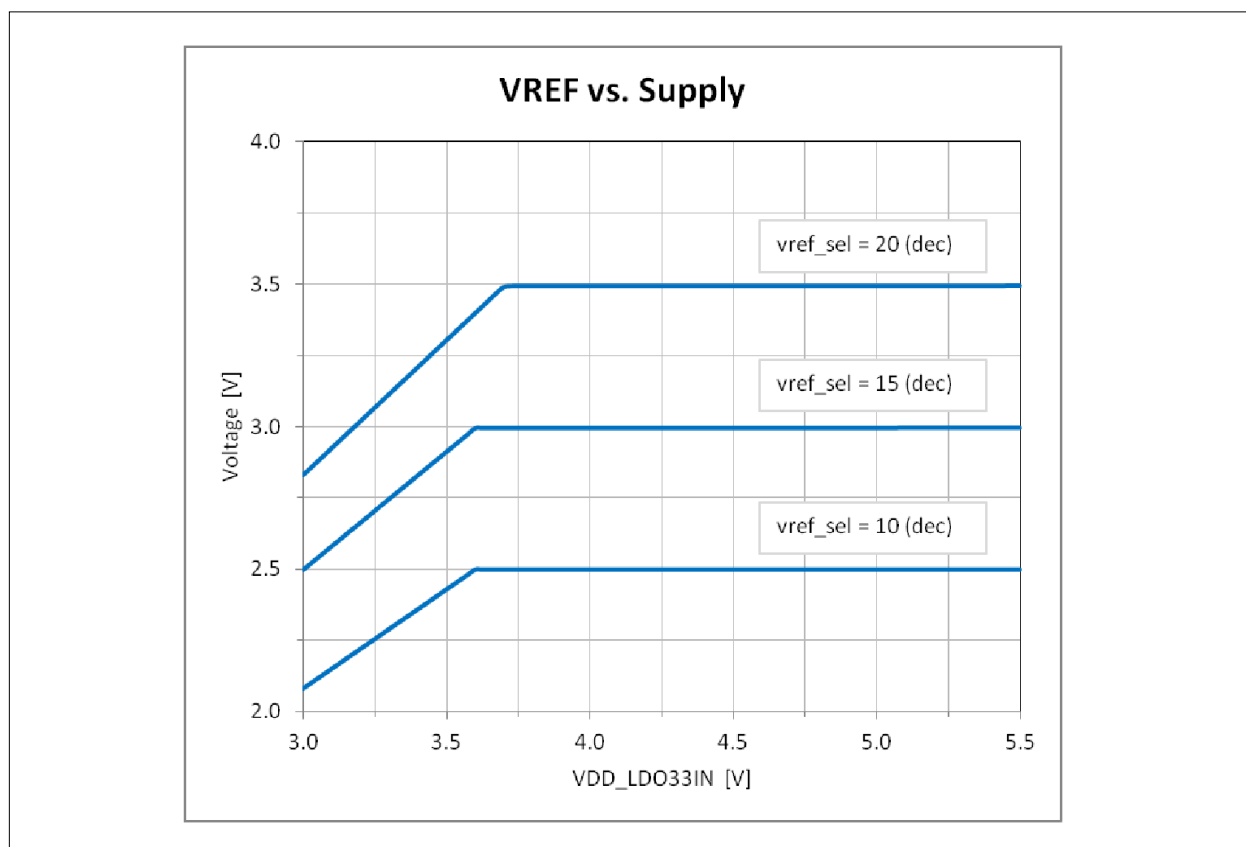


Figure 19: VREF vs Input Supply

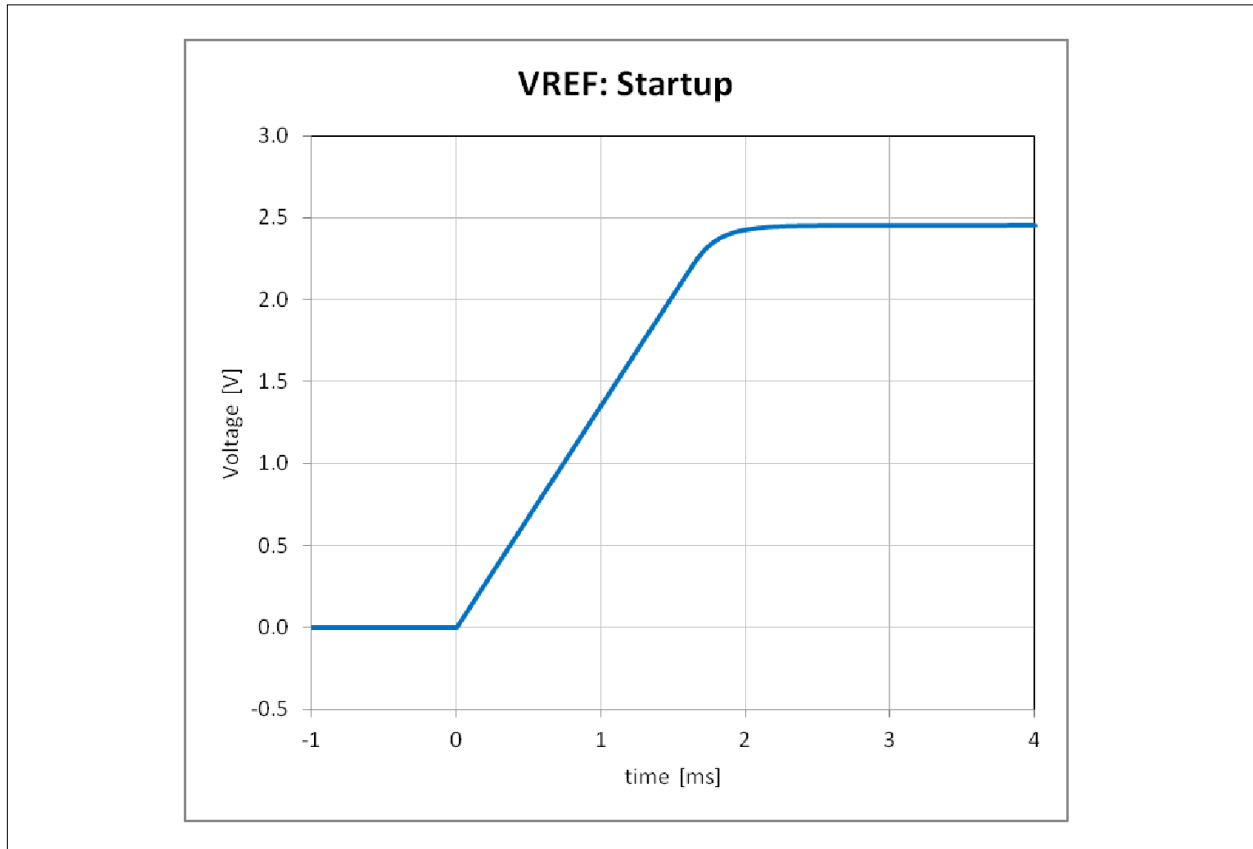


Figure 20: VREF Startup

Analog LDO

Block Diagram

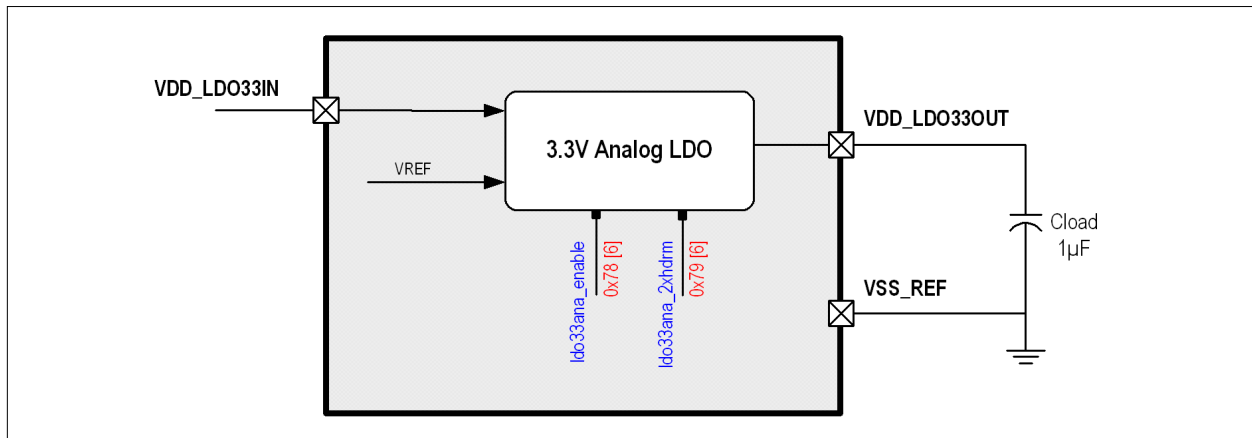


Figure 21: Analog LDO Block Diagram

Block Description

The analog LDO provides a clean supply rail for each microphone Rx chain, PGA + Anti-Aliasing Filter (AAF) + ADC, as well as each channel's associated VREF and current bias generators. This LDO accepts the programmable VREF signal as its input reference, and applies an inverse programming so that the output voltage is a constant 3.4V. A 50mA current limit is also implemented.

The cell also uses a minimum headroom scheme that maintains at least 5% or 10% of voltage headroom between the input VDD_LDO33IN supply and the output VDD_LDO33OUT—this supply tracking method ensures that even at low input supply voltages the PSRR of the LDO is not degraded.

Even if a system is running off only a 3.3V supply rail, the analog LDO should still be used as it automatically tracks the incoming 3.3V supply and generates either a 3.14V or 2.97V supply for the Rx channels.

Pin Description

For definitions of the I/O Type acronyms used in the following table, see "Signal Definitions" on page 34.

Table 27: Analog LDO Pin Description

Pin Label	Pin Number			I/O Type	Signal Name/Description
	CX20810-11Z	CX20811-11Z	CX20811-15Z		
VDD_LDO33IN	27	35	E3	PWR	Analog LDO Input Supply. 3V to 5.5V input—also the supply input for VREF and micbias generators.
VDD_LDO33OUT	28	36	E2	PWR	Analog LDO Output Supply. Nominally either a: • 3.4V with a 5V input • 3.14V with a 3.3V input The output tracks the input supply to maintain a selectable minimum headroom of 5% or 10%.
VSS_REF	33	42	C1	GND	Analog Reference GND. GND reference for the VREF generator and analog LDO.

Register Description

Table 28: REF_CTRL_1—0x78

Bits	Name	Default	R/W	Description
6	LDO33ANA_ENABLE	0	R/W	Enables the analog LDO: • 0 = Shuts down the LDO—there is 1.2mΩ resistance to GND at the output pin • 1 = Enables the LDO

Table 29: REF_CTRL_2—0x79

Bits	Name	Default	R/W	Description
6	LDO33ANA_2XHDM	0	R/W	Controls the minimum headroom between the analog LDO input and output. At the input supplies near the target output voltage, the output tracks lower to ensure good PSRR: • 0 = LDO headroom is 5% • 1 = LDO headroom is 10%
5	LDO33ANA_ILIM_DISABLE	0	R/W	Disable the output current that is limiting on the analog LDO: • 0 = Enables the 50mA current limit • 1 = Disables the current limit

Performance Data

Table 30: Analog LDO Specifications

Parameter	Minimum	Typical	Maximum	Units
Temperature	−40	27	125	°C
Supply Voltage—VDD_LDO33IN	3	5	5.5	V
Input VREF	1.5	—	4	V
Output Voltage—VDD_LDO33OUT	2.7	3.4	3.5	V
Clload	0.8	1	12	μF
ESR	—	—	0.2	Ω
Load Current	0	—	50	mA
Current Limit Threshold	50	—	—	mA
Output Noise (20Hz–20kHz)	—	−97	−90	dBV
PSRR (@ 1kHz)	−40	—	—	dB

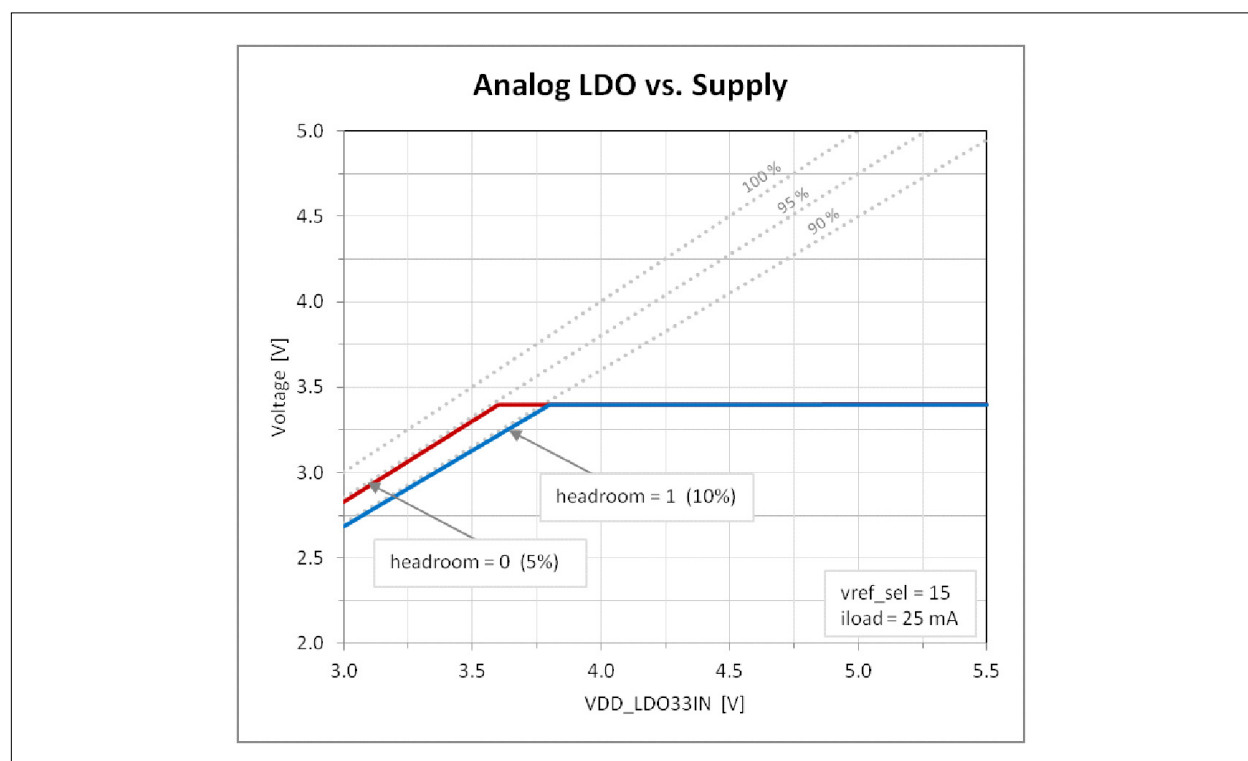


Figure 22: Analog LDO vs Input Supply

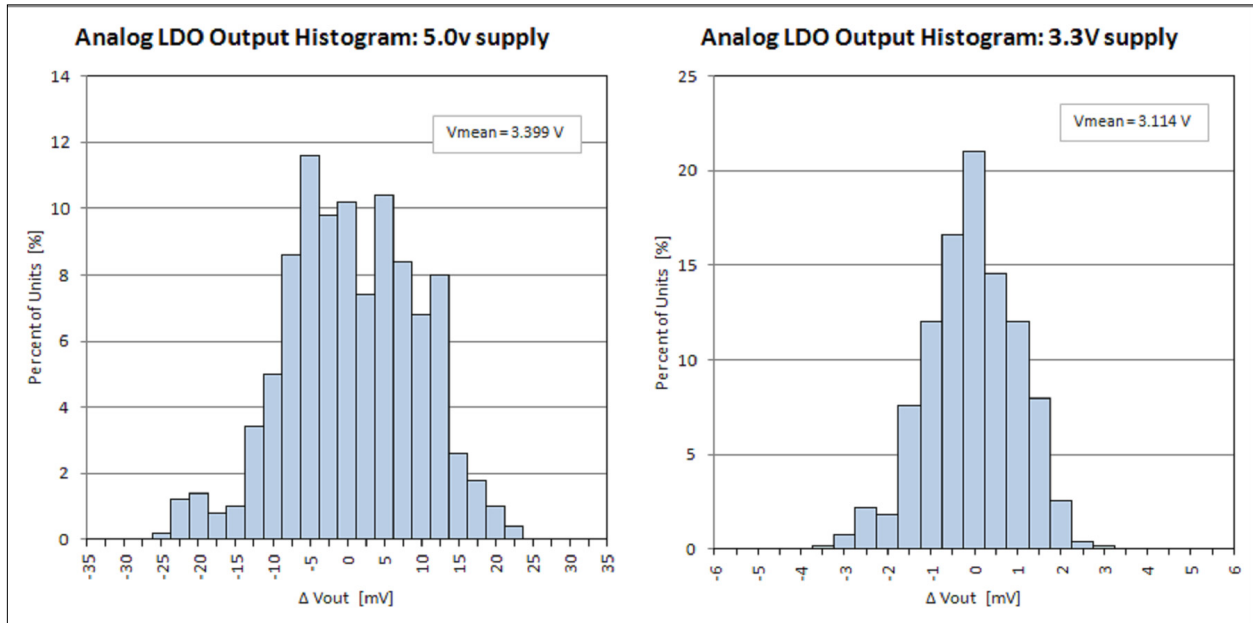


Figure 23: Analog LDO PSRR Output Histogram

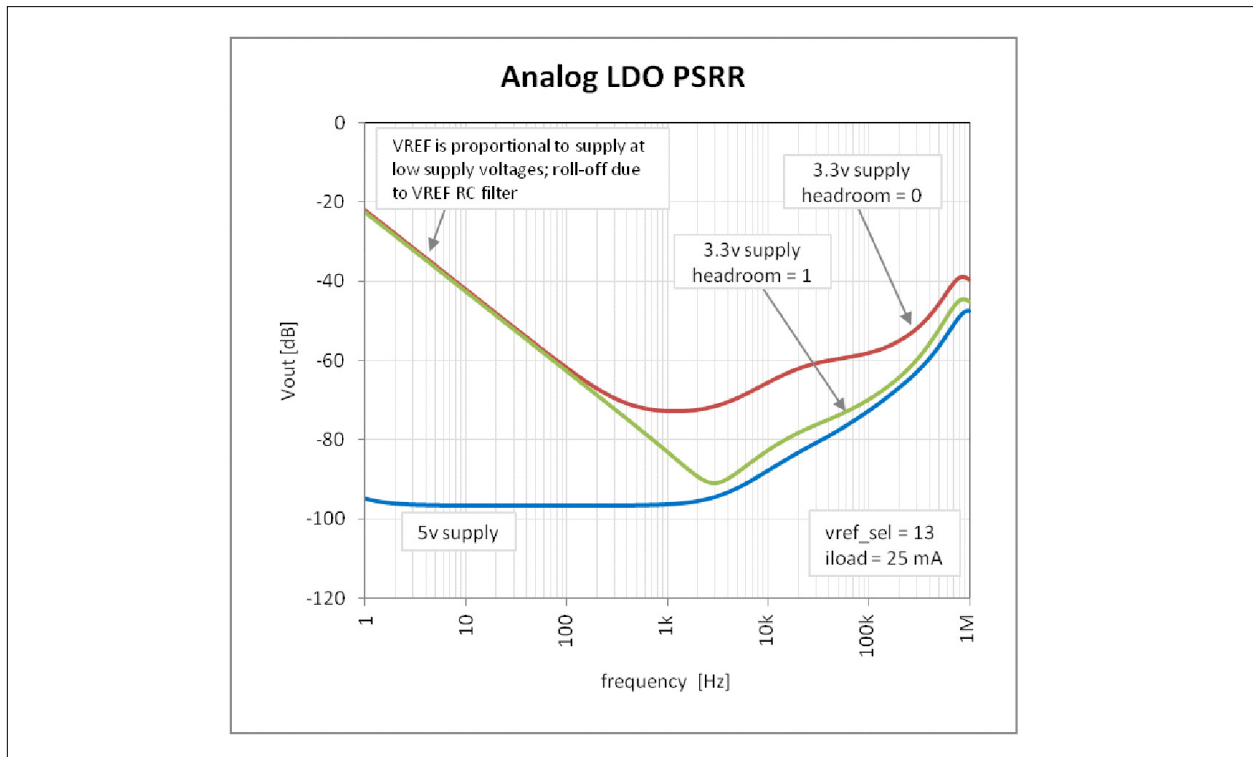


Figure 24: Analog LDO PSRR

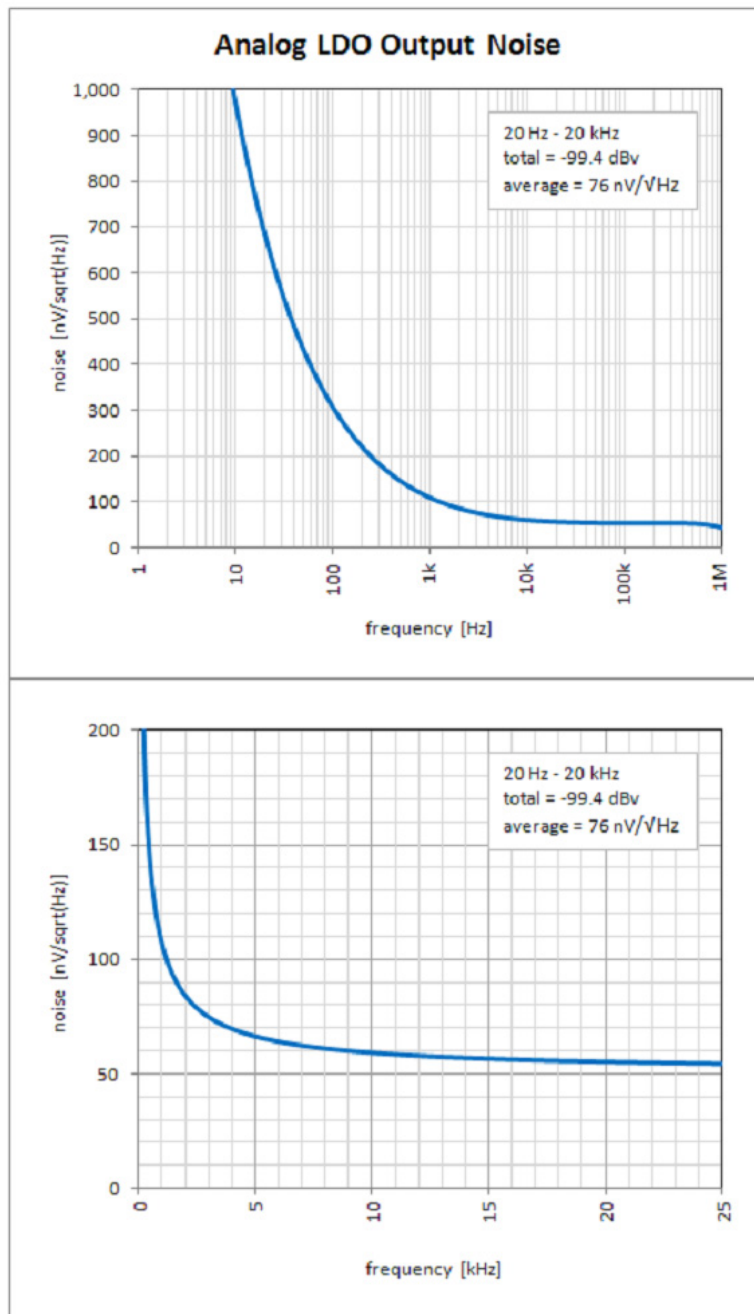


Figure 25: Analog LDO Output Noise

Power-On Resets (PORs)

The CX20810/CX20811 has the following three PORs:

- **POR_DIG33** = POR on 3.3V LDO33DIG_OUT. If LDO33DIG_OUT is low (below ~2.8V), the POR circuitry resets the CP. To reduce idle power consumption, this POR circuitry is self-biased and only enables itself when circuitry that uses its output signal is enabled (e.g., CP enabled, digital LDO enabled, PLL LDO enabled, etc.).
- **POR_VDD_CORE** = POR on the 1.2V VDD digital core. If VDD is low, the POR circuitry resets the digital core. The POR logic is a combination of the POR_VDD_CORE circuitry output and the CP state. If the CP is enabled, then the effective POR signal is an AND-ing of the CP ACTIVE signal (signifying that the CP has completed its weak soft-start phase and is currently in its high-power active state) and the POR_VDD_CORE circuitry output (~800mV worst-case threshold). This ensures that the digital core does not become active while the CP is still weakly ramping up its output voltage between 0.8V and 1.2V. If the CP is bypassed and its enable pin is held low, then the effective POR is just the POR_VDD_CORE circuitry output.
- **POR_PWM** = POR on the 3.3V PWM driver supply. If PVDD33_PWM is low (below ~2.4V), the PWM driver is disabled. To minimize idle power, this POR circuitry is only enabled when the PWM driver is enabled.

When either of the supplies is low (LDO33_DIGOUT or VDD), the analog-digital interface level shifters are disabled.

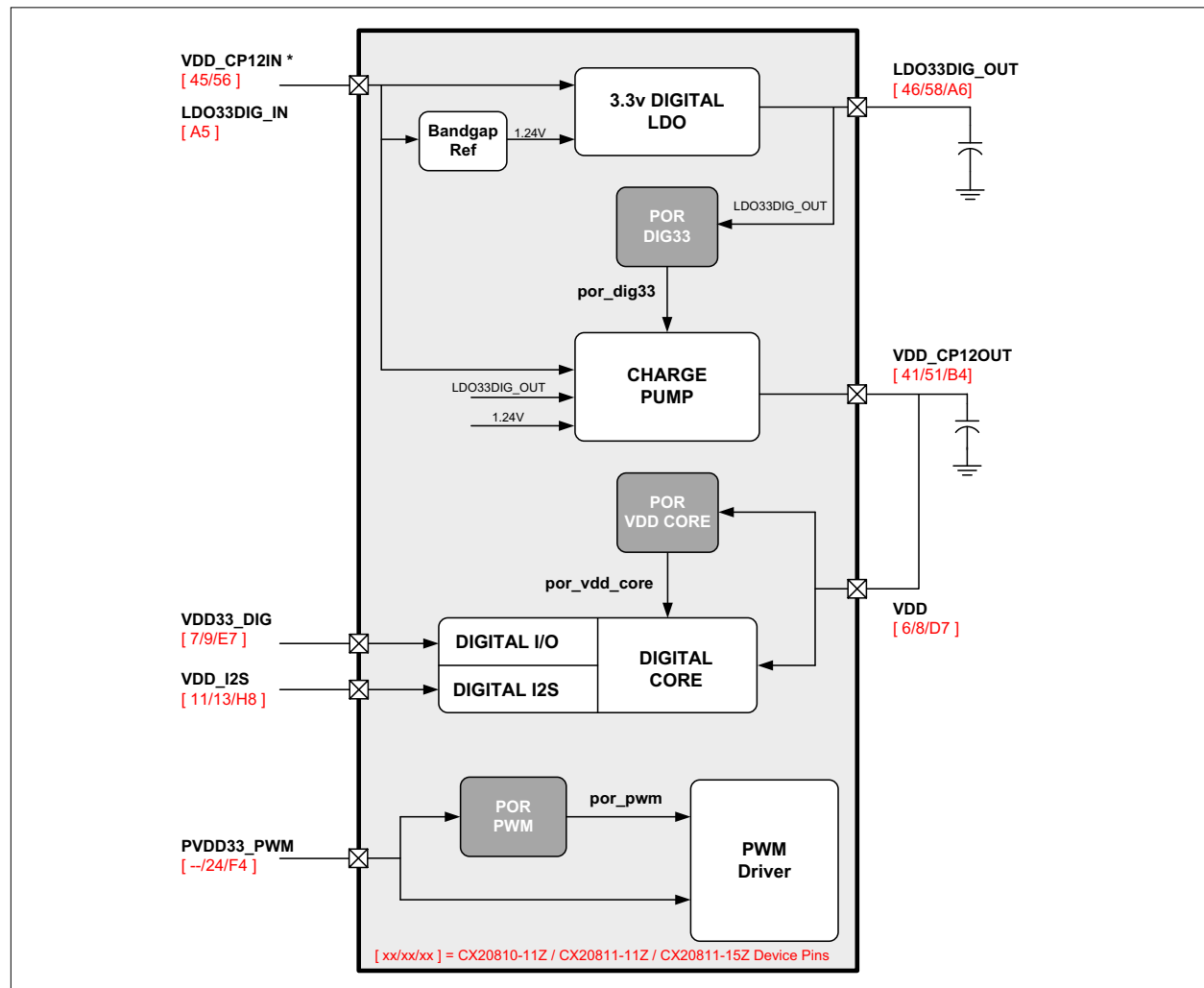


Figure 26: POR Reference Block Diagram

Microphone Receiver (Rx)

Block Diagram

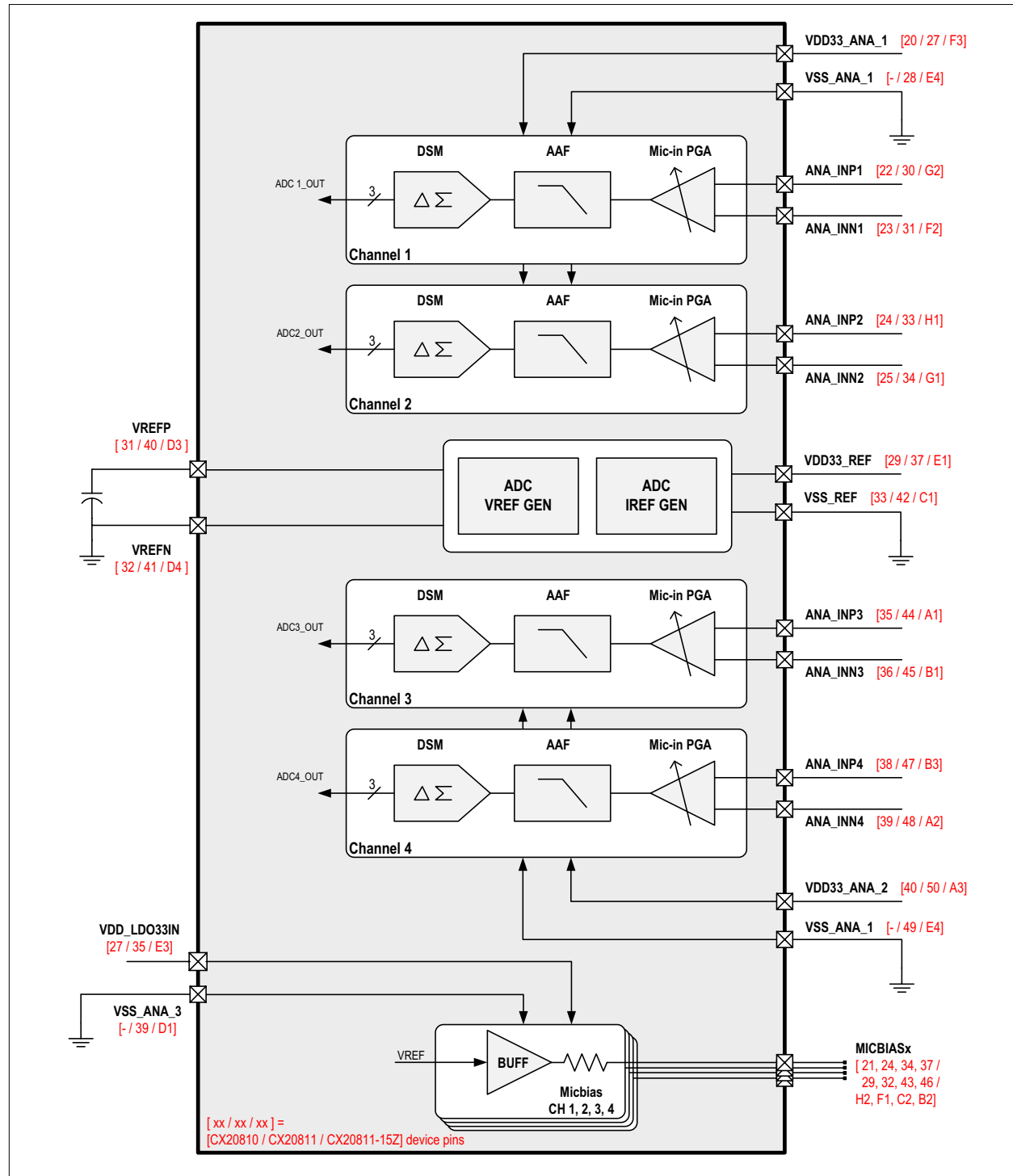


Figure 27: Microphone Rx Block Diagram

Overview

Each of the four high performance microphone receivers consists of a PGA, an AAF, a multi-bit Delta-Sigma Modulator (DSM) ADC, and a dedicated micbias amplifier. An ADC VREF and bias current generator is shared between the four receivers. Additional decimation, filtering, and mixing are performed in the digital domain.

Specifications

Table 31: Microphone Rx Specifications

Parameter	Minimum	Typical	Maximum	Units	Comments
Dynamic Range (A-weighted)	-		-	dBA	997Hz - Measured using a –60dBFS reference signal - A-weight filtering
PGA = 0dB		106			
PGA = 6dB		106			
PGA = 12dB		105			
PGA = 24dB		100			
PGA = 30dB		95			
Total Harmonic Distortion plus Noise (THD+N)	-		-	dBc	997Hz tone - The amount of distortion and noise with the audio band relative to the test signal - Tested at –1dBFS
PGA = 0dB		–89			
PGA = 6dB		–85			
PGA = 12dB		–85			
PGA = 24dB		–84			
PGA = 30dB		–84			
PSRR	-	90	-	dB	At 1kHz.
Crosstalk	-	90	-	dB	-
Input Resistance	-		-	kΩ	For gains = 3dB–30dB, the input resistance is programmable:
PGA = –6dB		16			500kΩ (default) 250kΩ 125kΩ 25kΩ
PGA = 0dB		8			
PGA = 3dB–30dB		500			

Note: Test conditions unless otherwise noted:

- $T_A = 27^{\circ}\text{C}$
- Input supply = 3.3V
- $F_s = 48\text{kHz}$
- MCLK = 12.288MHz (internal PLL is not used) or 24.000MHz (internal PLL used)

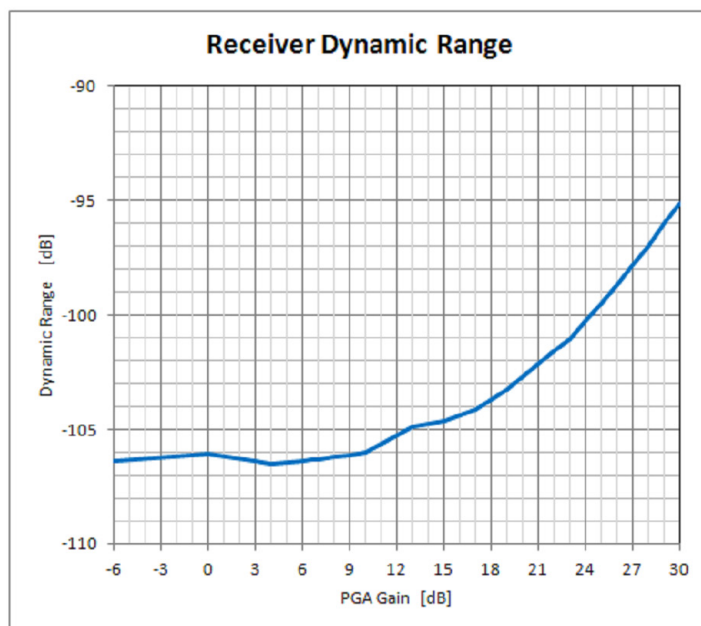


Figure 28: Rx Dynamic Range vs PGA Gain

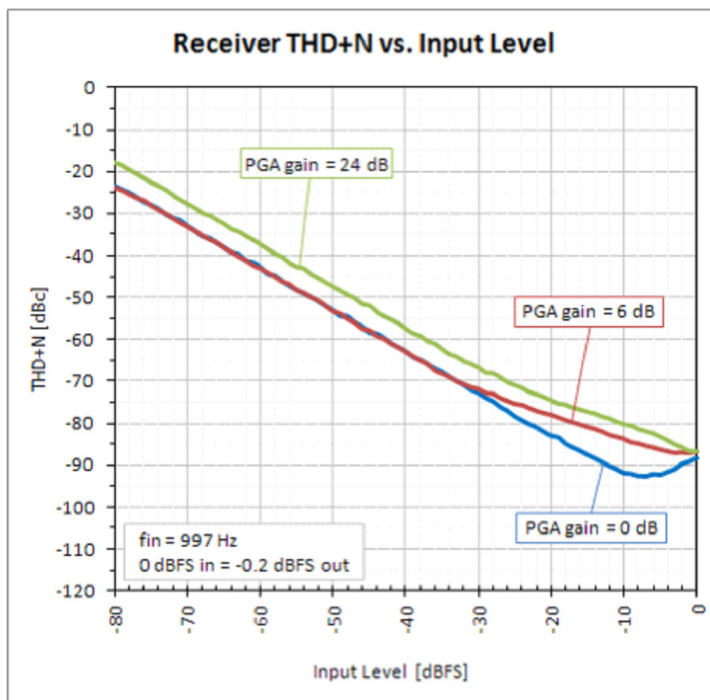


Figure 29: Rx THD+N vs Input Level

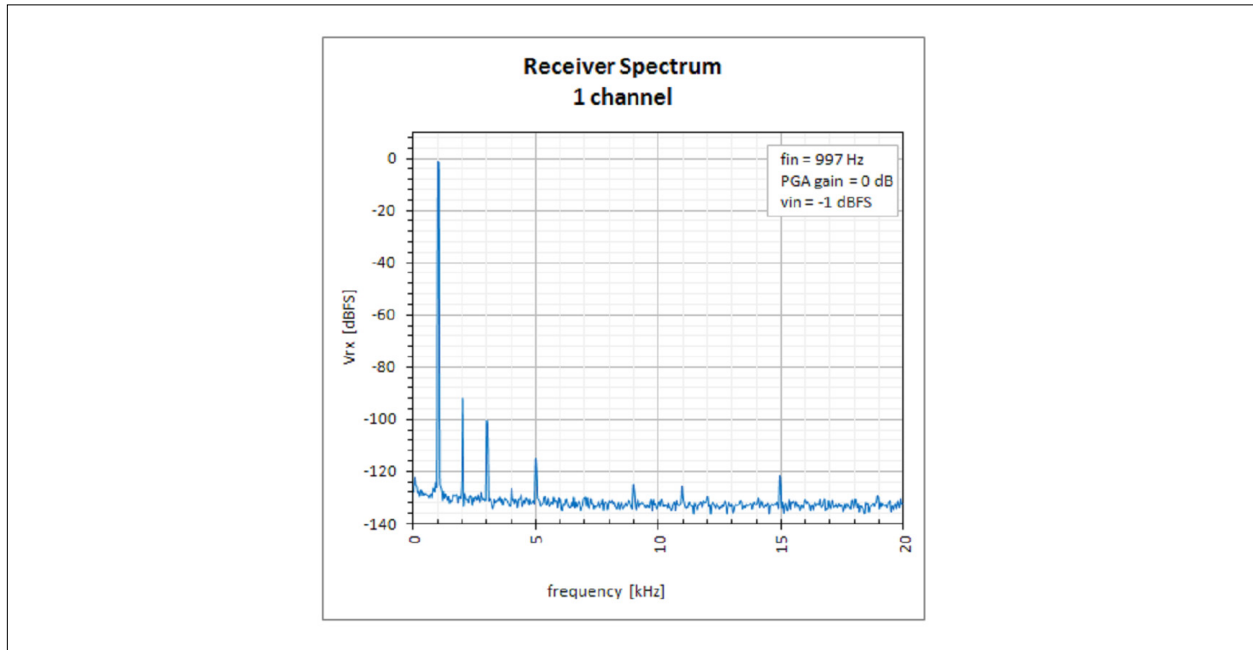


Figure 30: Rx Spectrum Plot, -1dBFS Input, PGA Gain = 0dB

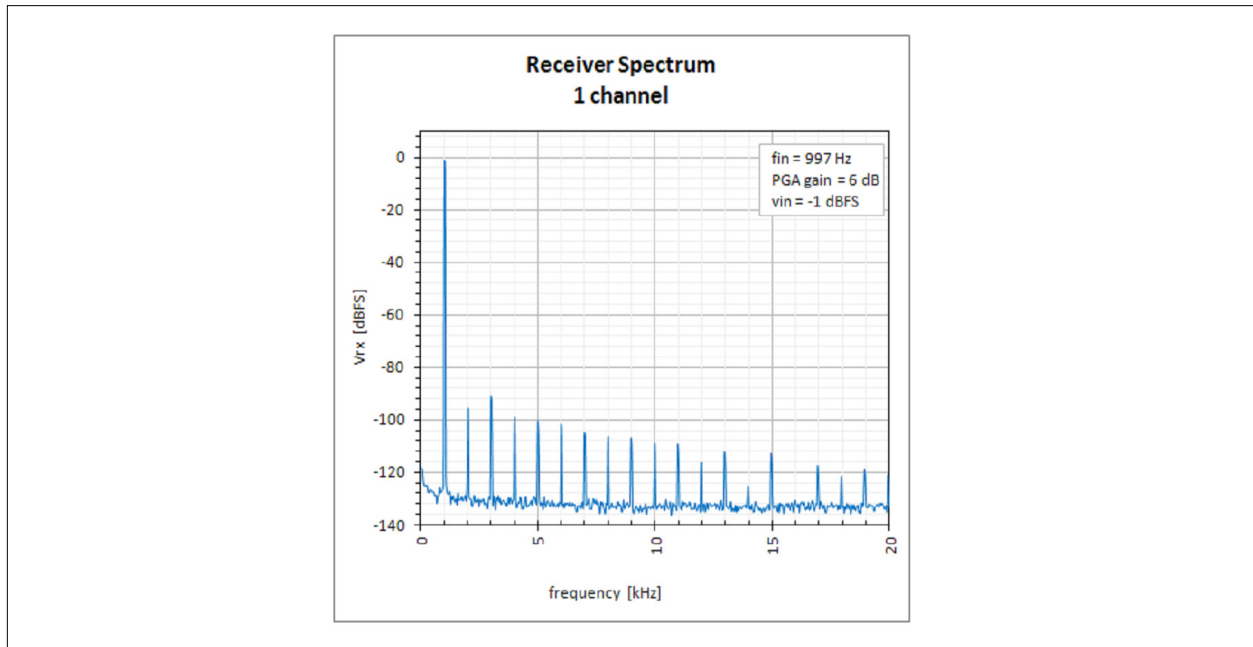


Figure 31: Rx Spectrum Plot, -1dBFS Input, PGA Gain = 6dB

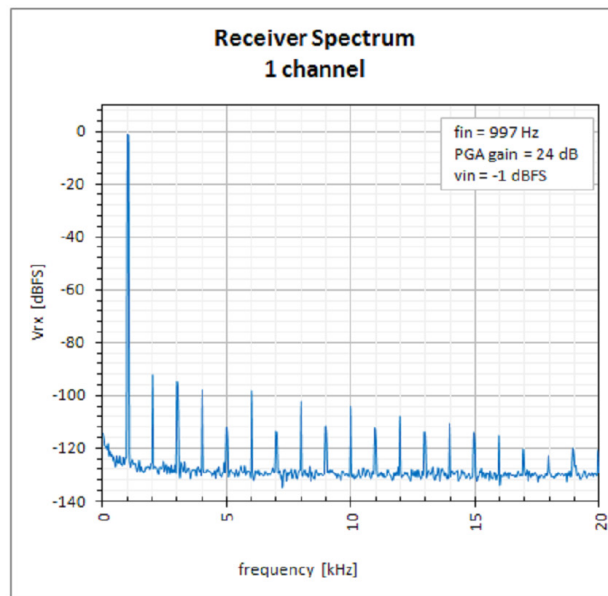


Figure 32: Rx Spectrum Plot, -1dBFS Input, PGA Gain = 24dB

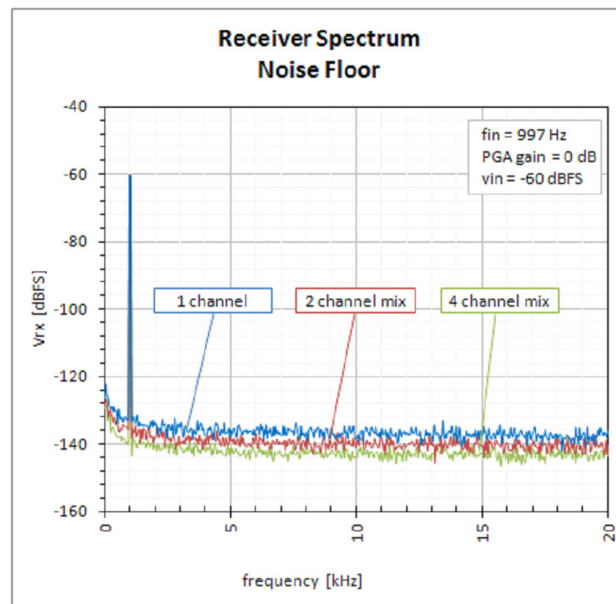


Figure 33: Rx Noise Floor Plots, -60dBFS Input, PGA Gain = 0dB, with Mixing

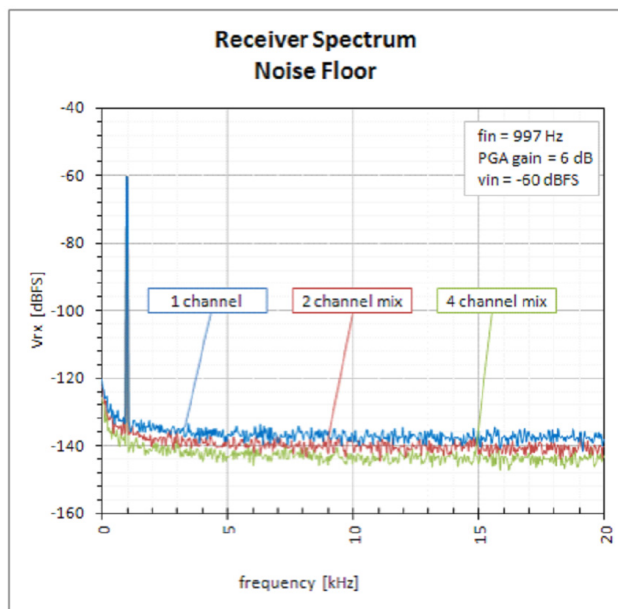


Figure 34: Rx Noise Floor Plots, -60dBFS Input, PGA Gain = 6dB, with Mixing

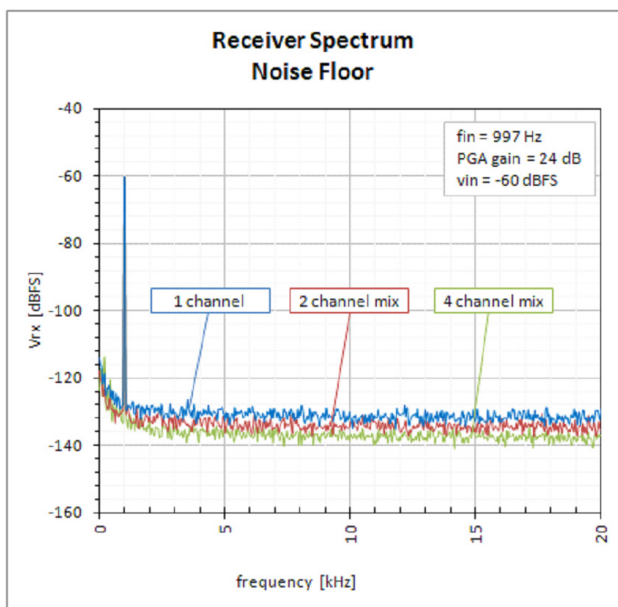


Figure 35: Rx Noise Floor Plots, -60dBFS Input, PGA Gain = 24dB, with Mixing

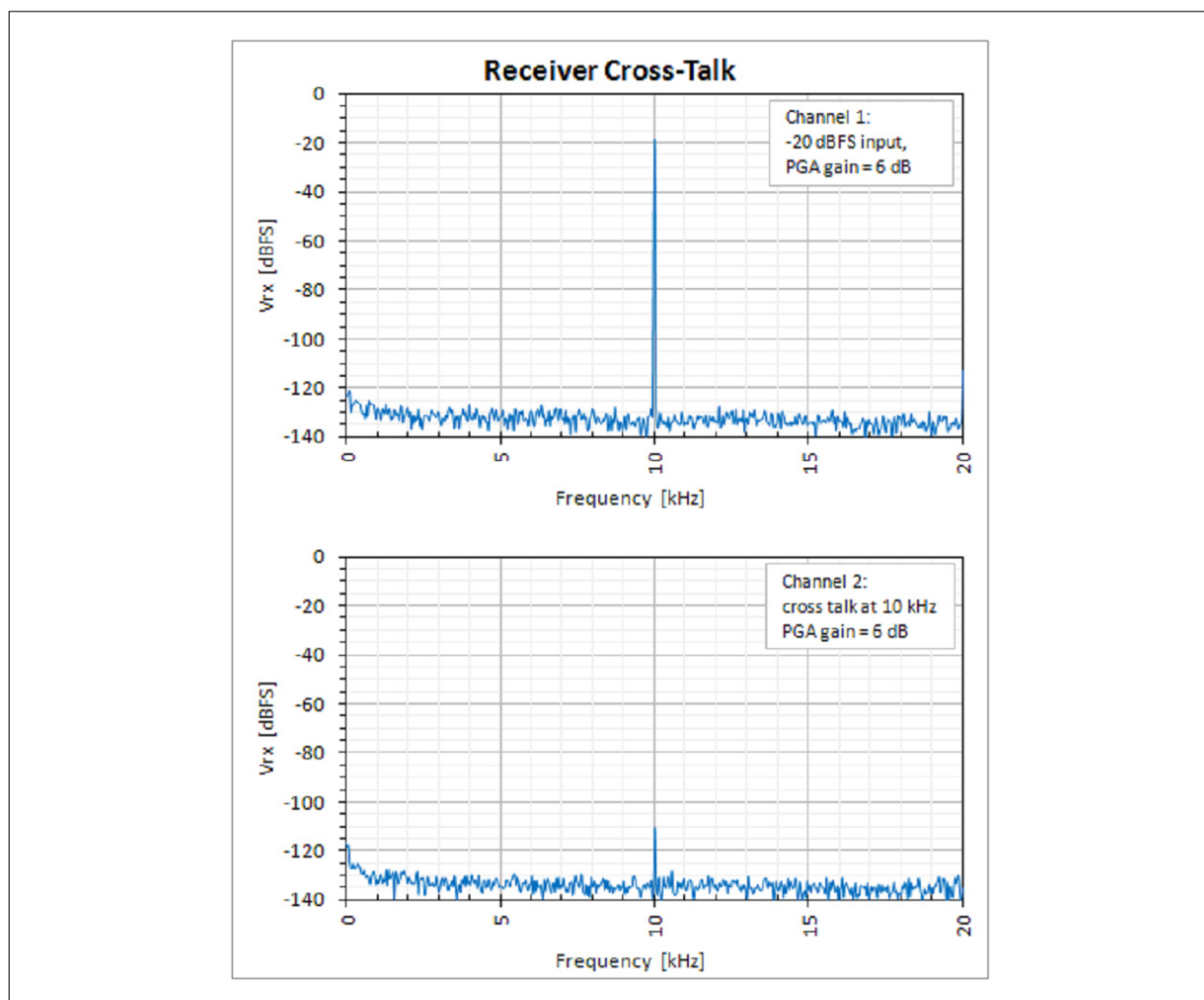


Figure 36: Rx Crosstalk

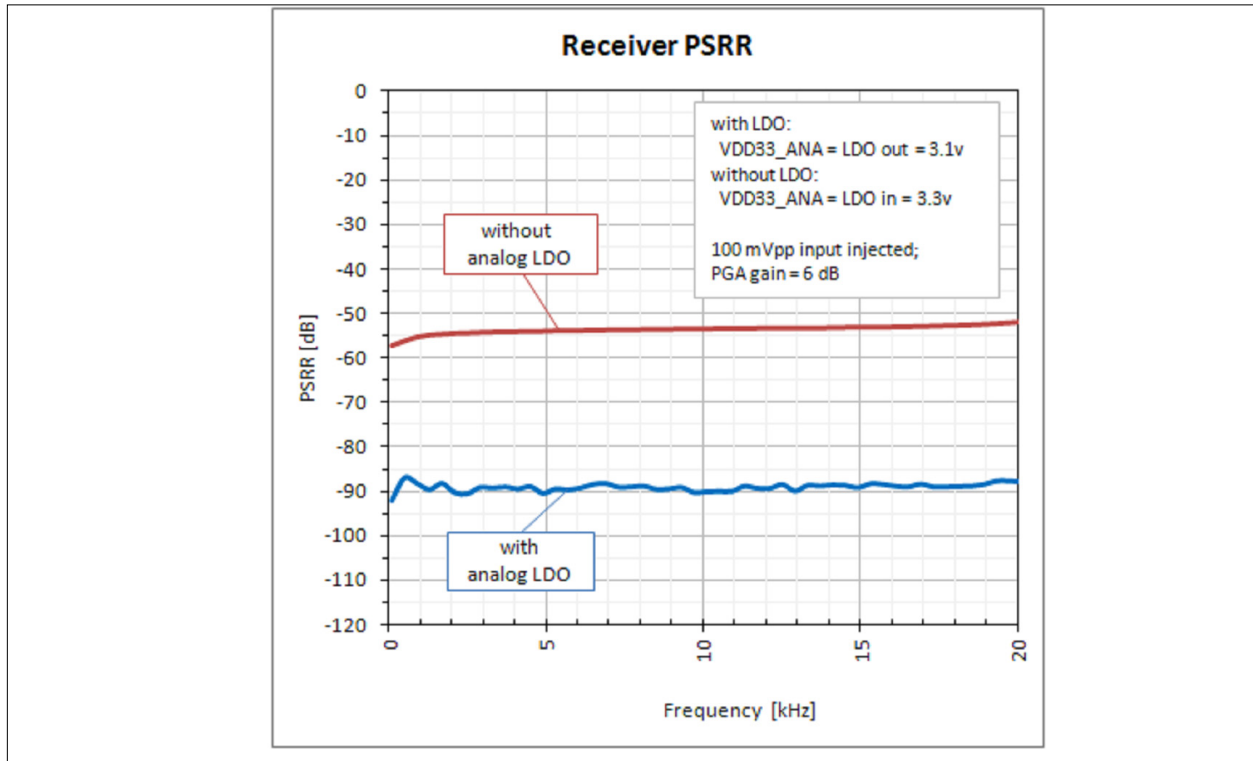


Figure 37: Rx PSRR

Note: The PSRR was measured by injecting a 100mV_{p-p} Alternating Current (AC) signal onto the analog LDO input (VDD_LDO33IN). When the analog LDO was enabled, the Rx's supply pin VDD33_ANA was connected to the LDO output (VDD_LDO33OUT). When the LDO was disabled, the VDD33_ANA pin was tied directly to the LDO input VDD_LDO33IN.

The PSRR is calculated by taking the ADC's digital output, converting it to an analog voltage, and then dividing that value by the input level (100mV_{p-p}).

Microphone Bias (Micbias)

Block Diagram

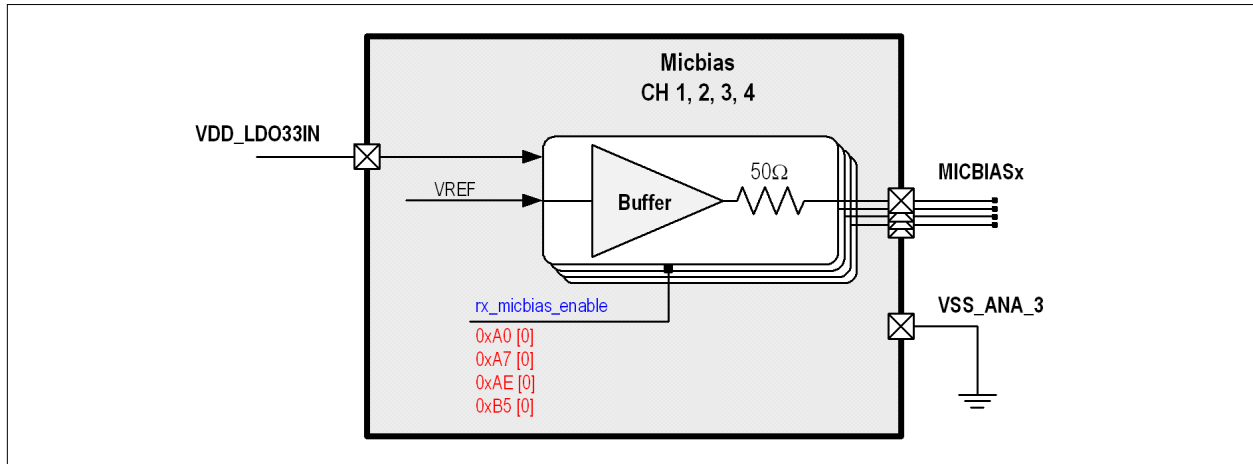


Figure 38: Micbias Block Diagram

Block Description

The micbias cell functions as a low-noise unity buffer that drives the VREF level onto the external electret type microphone. The amplifier has a 50Ω series output resistance, and an internal current limit of 10mA.

Pin Description

For definitions of the I/O Type acronyms used in the following table, see ["Signal Definitions"](#) on page 34.

Table 32: Micbias Pin Description

Pin Label	Pin Number			I/O Type	Signal Name/Description
	CX20810-11Z	CX20811-11Z	CX20811-15Z		
VDD_LDO33IN	27	35	E3	PWR	Analog LDO Input Supply. 3V to 5.5V input—also the supply input for VREF and micbias generators.
VSS_ANA_3	-	39	D1	GND	Analog GND. GND for the VREF, MICBIAS and bias current generators.
MICBIAS1	21	29	H2	Oa	ADC1 Micbias. Micbias output for channel 1.
MICBIAS2	24	32	F1	Oa	ADC2 Micbias. Micbias output for channel 2.
MICBIAS3	34	43	C2	Oa	ADC3 Micbias. Micbias output for channel 3.
MICBIAS4	37	46	B2	Oa	ADC4 Micbias. Micbias output for channel 4.
VREF	30	38	D2	Analog I/O	Analog VREF. Analog LDO and micbias VREF.
VSS_REF	33	42	C1	GND	Analog Reference GND. GND reference for the VREF generator and analog LDO.

Register Description

Table 33: ANA_ADC1_CTRL_1—0xA0

Bits	Name	Default	R/W	Description
0	RX1_MICBIAS_ENABLE	0	R/W	Channel 1 micbias enable: 0 = Shuts down the micbias 1 = Enables the micbias

Registers 0xA7, 0xAE, and 0xB5 similarly control channels 2, 3, and 4, respectively.

Performance Data

Table 34: Micbias Specifications

Parameter	Minimum	Typical	Maximum	Units
Temperature	–40	27	125	°C
Supply Voltage—VDD_LDO33IN	2.7	3.3/5	5.5	V
Input VREF	1.5	-	4	V
Output Voltage—Micbias	-	VREF	VDD_LDO33IN	V
Output Resistance	-	-	50	Ω
Output Load Current	-	-	10	mA
Output Noise (20Hz–20kHz)	-	11	-	nV/ $\sqrt{\text{Hz}}$
	-	–116	-	dBV
PSRR (@ 1kHz)	-	–85	–65	dB

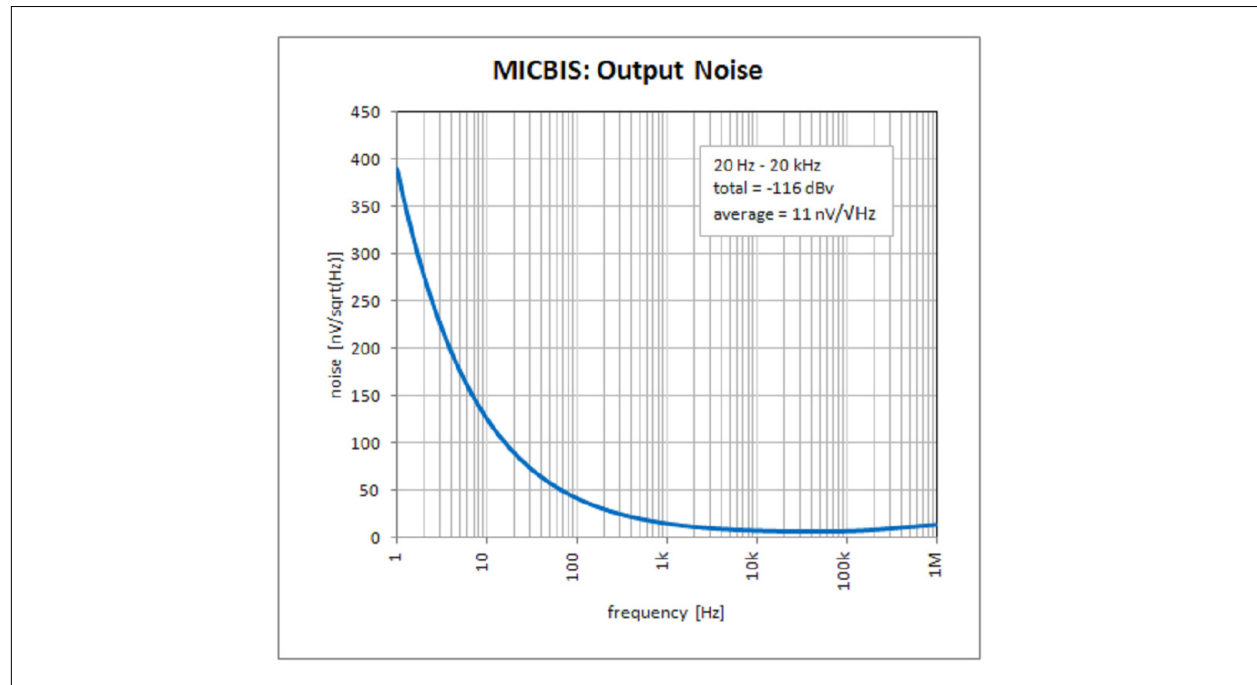


Figure 39: Micbias Output Noise

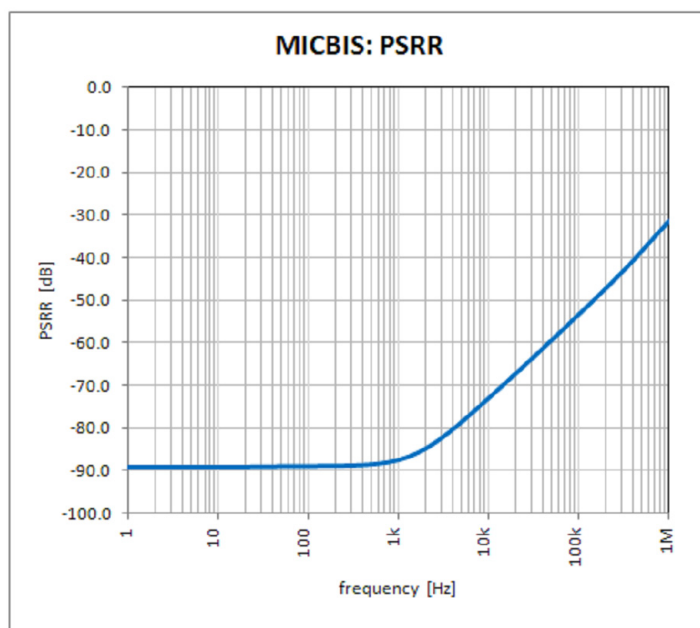


Figure 40: Micbias PSRR

Mic-In PGA

Block Diagram

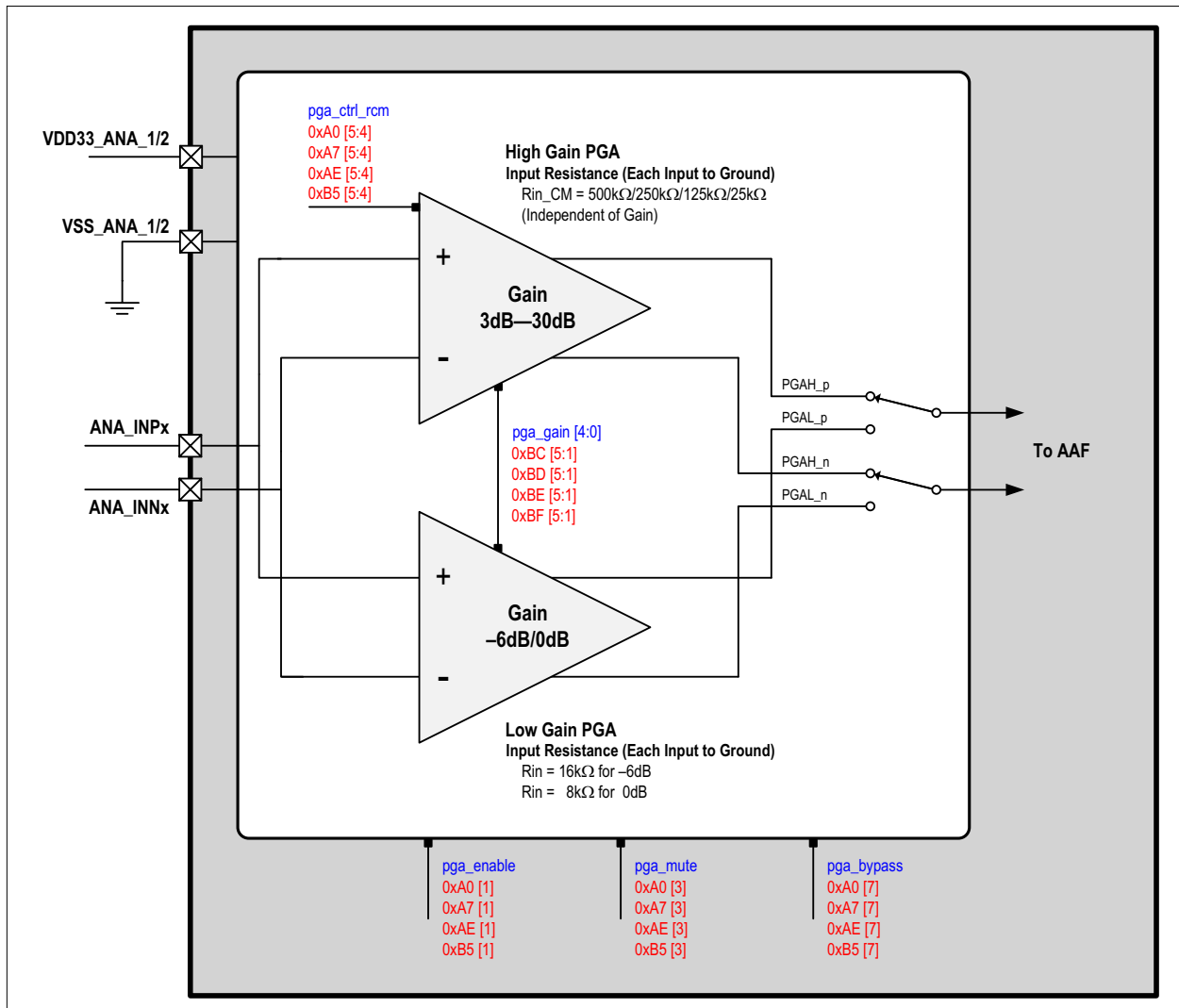


Figure 41: Mic-In PGA Block Diagram

Block Description

The mic-in PGA is a low noise, high linearity amplifier used to scale the incoming signal to achieve optimum performance. The PGA is designed to amplify input signals so that the maximum full-scale signal swing at the PGA output is $2V_{RMS}$. The gain programming is separated into two distinct modes of operation to address two different applications:

- High gain mode = Intended for microphone applications, the gain is programmable from 3dB to 30dB in 1dB steps (an additional 0.5dB step is available in the AAF; see register 0xBC [0]). The impedance seen at the input pins is selectable using pga_ctrl_rcm (register 0xA0 [5:4]): 500k Ω (default), 250k Ω , 125k Ω , or 25k Ω .
- Low gain mode = Intended for line-input applications, the gain is selectable between -6dB and 0dB only. When in these two gain settings, the input impedance is either 16k Ω (-6dB setting) or 8k Ω (0dB setting).

An additional high performance line-in bypass mode is included, which bypasses the PGA completely and routes the ANA_INP and ANA_INN signals directly into the AAF and ADC with 0dB gain. This mode is selectable using pga_bypass (see register 0xA0 [7]).

The PGA design also optimizes power consumption through advanced adaptive biasing and tracking schemes. This circuitry automatically adjusts the PGA's internal bias currents and node voltages based on the incoming signal to minimize bias overhead, while maintaining high linearity and noise performance.

Another advanced feature implemented in the PGA is an offset calibration mechanism. Due to varying offsets for each gain setting, the offset of each channel and gain setting is measured and zeroed out so that gain transitions do not result in an audible *click*. This calibration can be run either automatically across all of a channel's gain settings, or it can be run individually on just a particular PGA setting. Calibration on a particular gain setting takes approximately 60 μ s, while calibrating all of the gain settings on a channel takes about 1.8ms. Because each channel has its own dedicated calibration engine that can run in parallel, all of the channels can be calibrated in 1.8ms.

Pin Description

For definitions of the I/O Type acronyms used in the following table, see ["Signal Definitions"](#) on page 34.

Table 35: MIC IN Pin Description

Pin Label	Pin Number			I/O Type	Signal Name/Description
	CX20810-11Z	CX20811-11Z	CX20811-15Z		
VDD33_ANA_1	20	27	F3	PWR	Microphone 1 and 2 Paths Analog Supply Pin. Connect to the analog LDO (VDD_LDO33OUT)
VSS_ANA_1	-	28	E4	GND	Microphone 1 and 2 Paths GND. Analog GND to ADC1 and ADC2 paths.
ANA_INP1	22	30	G2	Ia	ADC1 Positive Input. Positive microphone input signal for channel 1.
ANA_INN1	23	31	F2	Ia	ADC1 Negative Input. Negative/GND-sense microphone input signal for channel 1.
ANA_INP2	25	33	H1	Ia	ADC2 Positive Input. Positive microphone input signal for channel 2.
ANA_INN2	26	34	G1	Ia	ADC2 Negative Input. Negative/GND-sense microphone input signal for channel 2.
VDD33_ANA_2	40	50	A3	PWR	Microphone 3 and 4 Paths Analog Supply Pin. Connect to the analog LDO (VDD_LDO33OUT)
VSS_ANA_2	-	49	C3	GND	Microphone 3 and 4 Paths GND. Analog GND to ADC3 and ADC4 paths.
ANA_INP3	35	44	A1	Ia	ADC3 Positive Input. Positive microphone input signal for channel 3.
ANA_INN3	36	45	B1	Ia	ADC3 Negative Input. Negative/GND-sense microphone input signal for channel 3.
ANA_INP4	38	47	B3	Ia	ADC4 Positive Input. Positive microphone input signal for channel 4.
ANA_INN4	39	48	A2	Ia	ADC4 Negative Input. Negative/GND-sense microphone input signal for channel 4.

PGA Register Description

Table 36: ANA_ADC1_CTRL_1—0xA0

Bits	Name	Default	R/W	Description
7	RX1_PGA_BYPASS	0	R/W	Channel 1 PGA bypass for line-in mode: 0 = Does not bypass the PGA path 1 = Bypasses the PGA and routes the inputs directly into the AAF with 0dB gain
6	RX1_PGA_BYP_RCM	0	R/W	Channel 1 PGA common-mode input resistance shorting: 0 = Does not short the resistance 1 = Shorts the resistance to speed-up the capacitor charging
5:4	RX1_PGA_CTRL_RCM	0	R/W	Channel 1 high-gain PGA input impedance control: 0 = 500kΩ 1 = 250kΩ 2 = 125kΩ 3 = 25kΩ
3	RX1_PGA_MUTE	0	R/W	Channel 1 PGA mute control: 0 = PGA in normal mode 1 = Disconnects the input pins and shorts the PGA inputs to the bias
1	RX1_PGA_ENABLE	0	R/W	Enables the channel 1 PGA: 0 = Shuts down the PGA 1 = Enables the PGA

Registers 0xA7, 0xAE, and 0xB5 similarly control channels 2, 3, and 4, respectively.

Table 37: ADC1_ANALOG_PGA_GAIN—0xBC

Bits	Name	Default	R/W	Description
5:1	RX1_ANALOG_PGA [5:1]	0	R/W	Channel 1 PGA settings: • 0 = 0dB • 1 = -6dB • 2 = 3dB • 3 = 3dB • 4 = 4dB • 5 = 5dB • 6 = 6dB • 7 = 7dB • 8 = 8dB • 9 = 9dB • 10 = 10dB • 11 = 11dB • 12 = 12dB • 13 = 13dB • 14 = 14dB • 15 = 15dB • 16 = 16dB • 17 = 17dB • 18 = 18dB • 19 = 19dB • 20 = 20dB • 21 = 21dB • 22 = 22dB • 23 = 23dB • 24 = 24dB • 25 = 25dB • 26 = 26dB • 27 = 27dB • 28 = 28dB • 29 = 29dB • 30 = 30dB • 31 = 31dB Refer to the "PGA" section in the <i>CX20810/CX20811 Data Sheet</i> for additional information on peak input level per gain setting.
0	RX1_ANALOG_PGA [0]	0	R/W	Channel 1 PGA 0.5dB step (implemented in AAF): • 0 = 0.0dB • 1 = 0.5dB

Registers 0xBD, 0xBE, and 0xBF similarly control channels 2, 3, and 4, respectively.

Gain Control

Table 38: PGA Gain Setting

pga_gain [4:0] (decimal)	Gain Setting (dB)	Output-Referred Gain (dB)	Maximum Input Level (V_{RMS} diff)	Output Level (V_{RMS} diff)	Input Resistance (k Ω)
0	0	6	1.000	2	8
1	-6	0	2.000	2	16
2	3	9	0.501	1.4125	500/250/125/25
3	3	9	0.501	1.4125	500/250/125/25
4	4	10	0.501	1.5849	500/250/125/25
5	5	11	0.501	1.7783	500/250/125/25
6	6	12	0.501	2	500/250/125/25
7	7	13	0.447	2	500/250/125/25
8	8	14	0.398	2	500/250/125/25
9	9	15	0.355	2	500/250/125/25
10	10	16	0.316	2	500/250/125/25
11	11	17	0.282	2	500/250/125/25
12	12	18	0.251	2	500/250/125/25
13	13	19	0.224	2	500/250/125/25
14	14	20	0.200	2	500/250/125/25
15	15	21	0.178	2	500/250/125/25
16	16	22	0.159	2	500/250/125/25
17	17	23	0.141	2	500/250/125/25
18	18	24	0.126	2	500/250/125/25
19	19	25	0.112	2	500/250/125/25
20	20	26	0.100	2	500/250/125/25
21	21	27	0.089	2	500/250/125/25
22	22	28	0.079	2	500/250/125/25
23	23	29	0.071	2	500/250/125/25
24	24	30	0.063	2	500/250/125/25
25	25	31	0.056	2	500/250/125/25
26	26	32	0.050	2	500/250/125/25
27	27	33	0.045	2	500/250/125/25
28	28	34	0.040	2	500/250/125/25
29	29	35	0.036	2	500/250/125/25
30	30	36	0.032	2	500/250/125/25
31	30	36	0.032	2	500/250/125/25

Note: The PGA output referred gain = gain setting + 6dB due to the SE to differential conversion. The 3dB, 4dB, and 5dB gain setting maximum inputs are fixed at $0.501V_{RMS}$ to maintain high linearity.

External Input Configurations

Because the Rx is designed to support microphones as well as line input signals, Synaptics recommends different input configurations. The diagrams in this section give suggested configurations for each case.

There is a change in the Direct Current (DC) blocking capacitor values when going from the high PGA settings in the microphone applications to the low PGA settings in the line input applications. Due to the differences in input impedance, a larger capacitor is needed for the low gain settings to maintain a low enough high pass cut-off frequency.

See "Anti-Aliasing Filter (AAF)" on page 102 for a more detailed analysis on the effects of the external LPF between the microphone or line input signal and the devices. The C_{AAF} capacitor can be optimized as a function of the source resistance (microphone resistance + bias resistor + filter series resistors) and desired filtering at the ADC clock frequency.

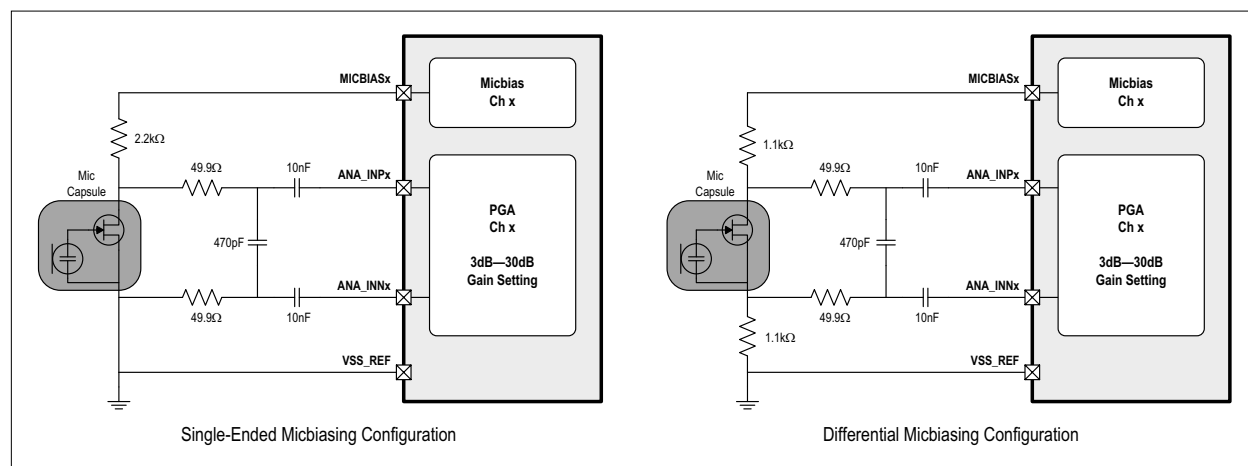


Figure 42: Microphone Configurations

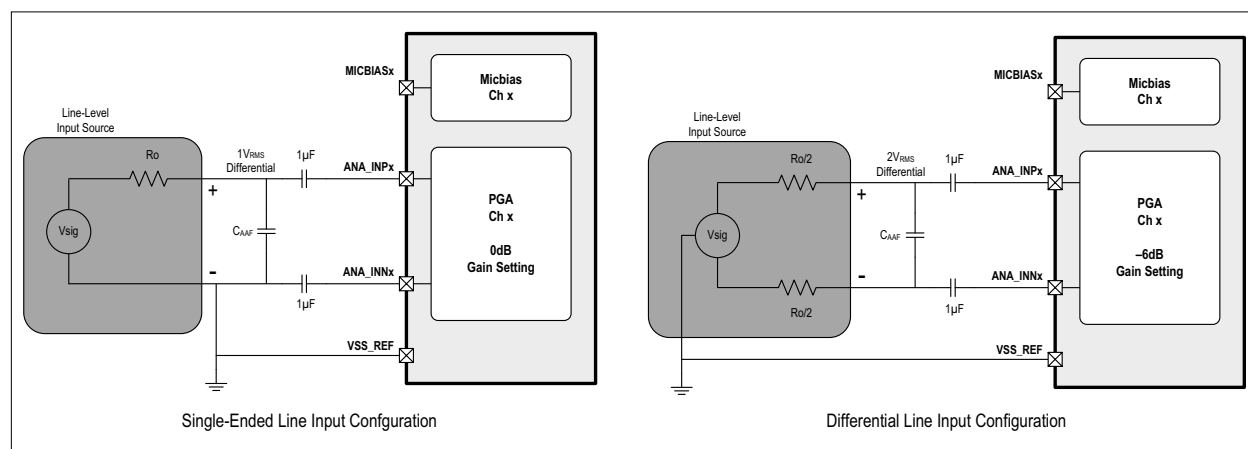


Figure 43: Line Input Configurations

Calibration

Due to PGA output offsets that vary randomly with the gain, gain transitions can result in audible clicks in the Rx signal. The CX20810/CX20811 implements off-line offset calibration on each channel and for each gain setting. This section details the basic scheme and procedure to initiate calibration.

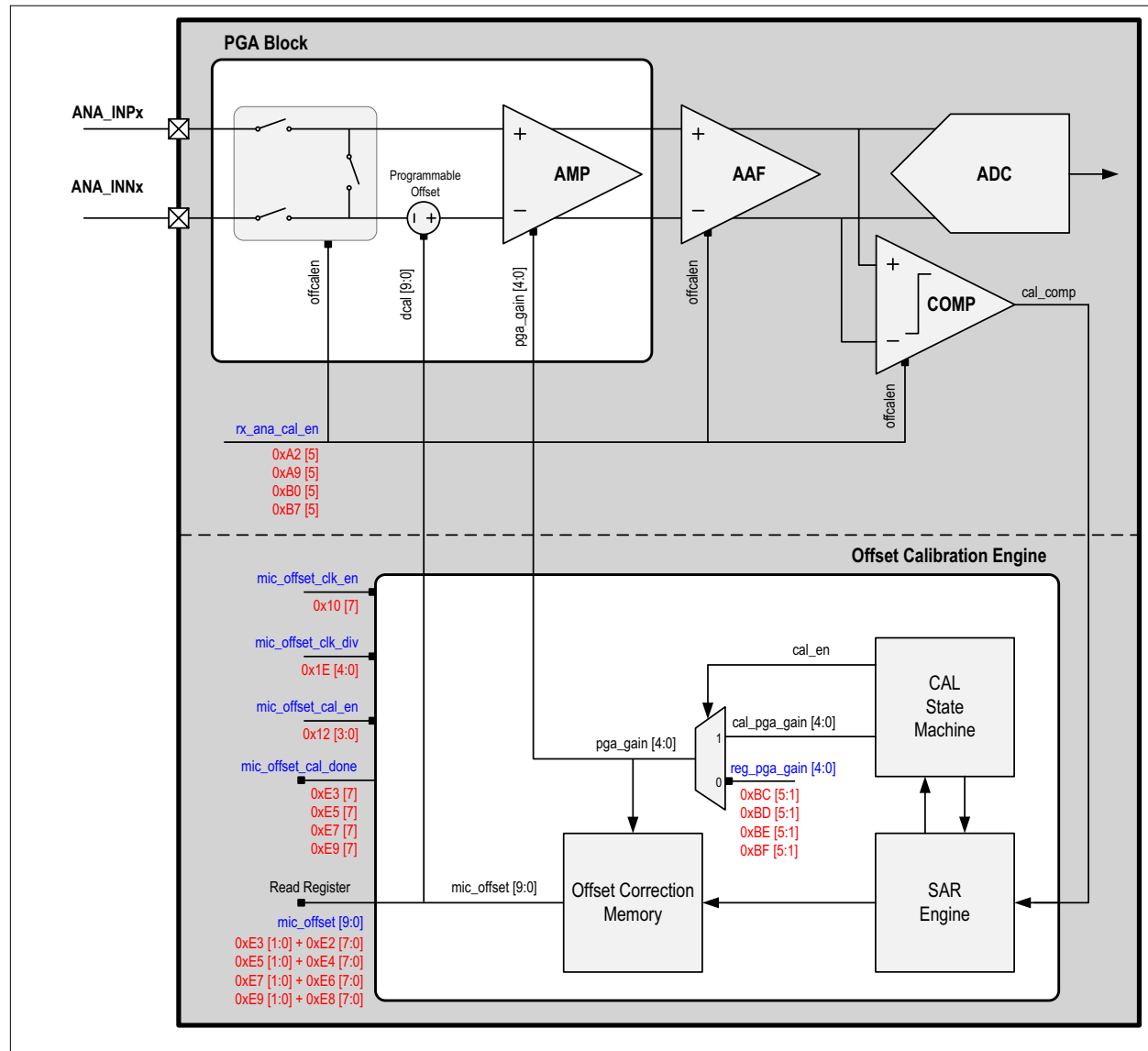


Figure 44: Rx Offset Calibration Block Diagram

The calibration involves shorting the PGA's inputs together and measuring the output offset. The AAF is reconfigured into a pre-amplifier to scale up the PGA's output offset, and a test comparator is used to determine the polarity of the resulting amplified offset. The comparator output is used by a digital Successive-Approximate Register (SAR) engine to do a binary search of the systematic offset needed at the PGA's input to minimize the measured offset. The resulting optimal code is stored in an offset correction table. This search and code storage is then applied to each of the PGA's gain setting.

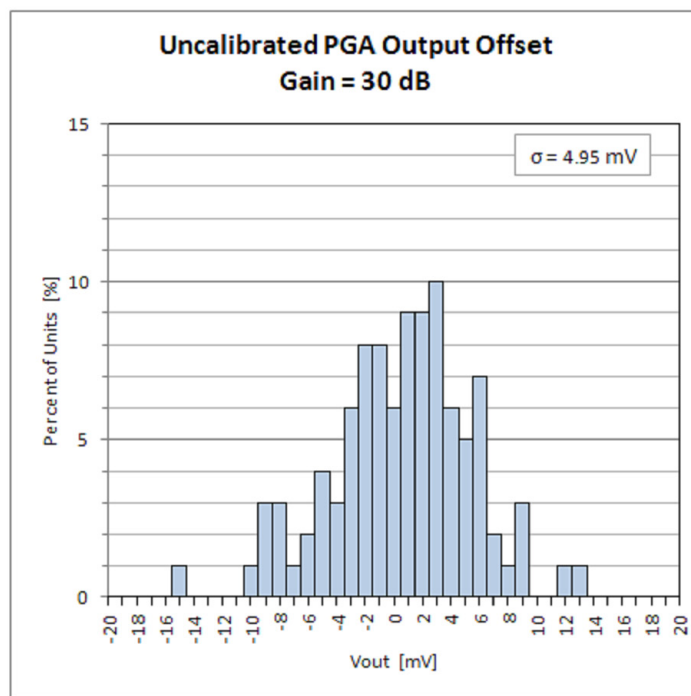


Figure 45: Uncalibrated PGA Output Offset—Gain = 30dB

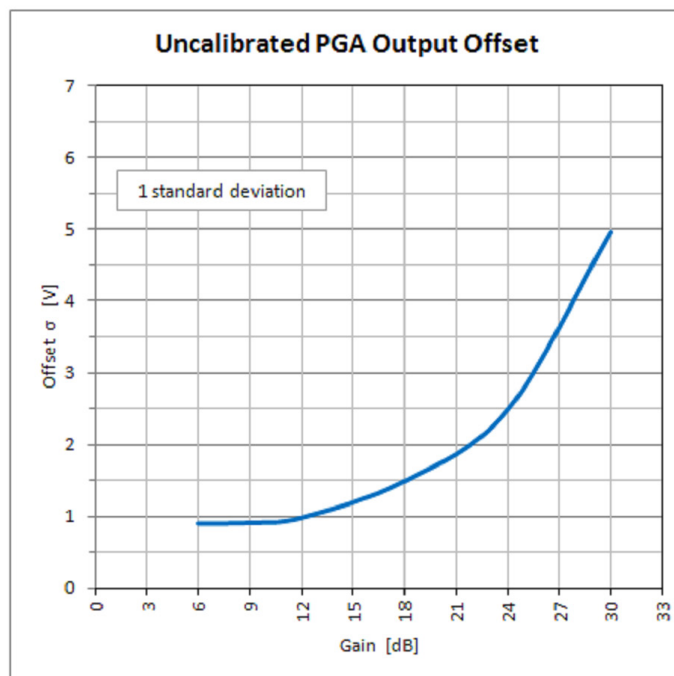


Figure 46: Uncalibrated PGA Output Offset

The programmable offset circuitry implemented in the PGA's input is controlled by a 10-bit calibration code, where the Most Significant Bit (MSB) is a polarity bit and the lower nine bits control the magnitude. The following figures show that the maximum input correction range is $\pm 7\text{mV}$, while the calibration resolution is approximately $14\mu\text{V}$. For the maximum PGA of 30dB, this translates into a worst-case residual output offset of less than $500\mu\text{V}$.

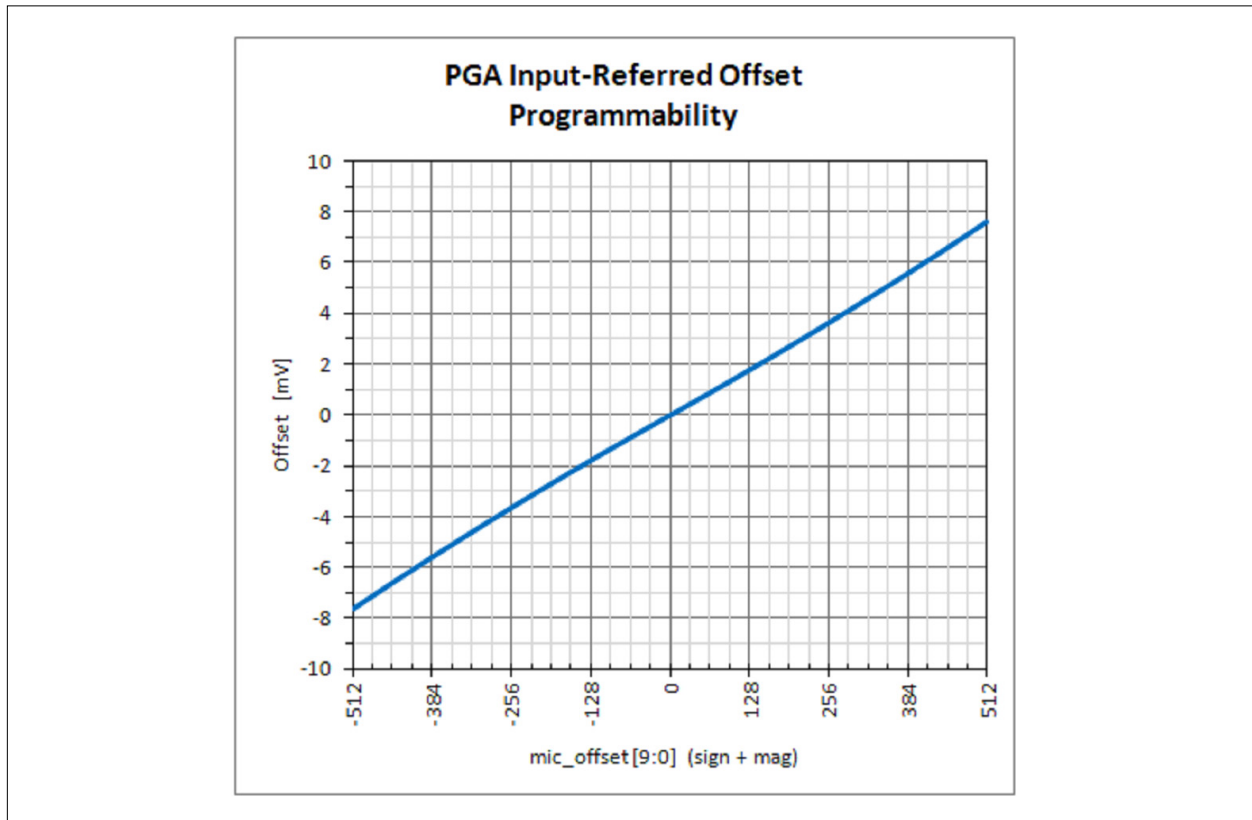


Figure 47: PGA Input Offset Programmability

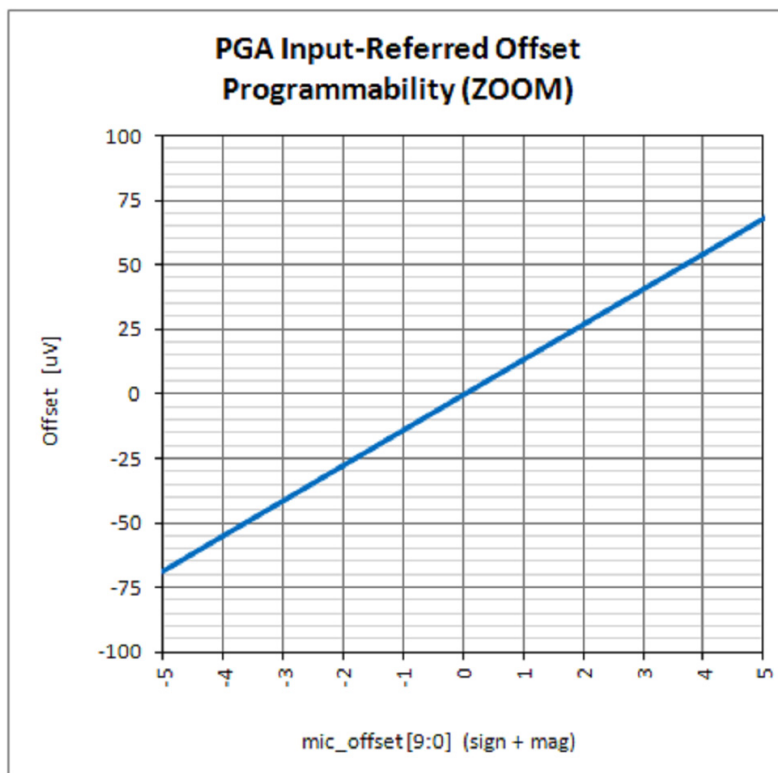


Figure 48: PGA Input Offset Programmability (ZOOM)

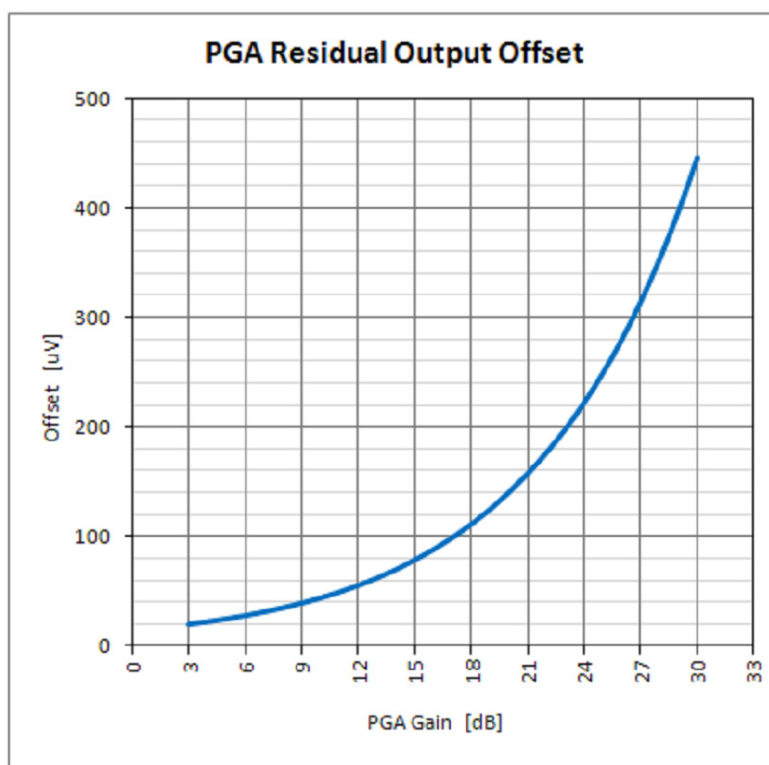


Figure 49: Worst-Case Calibrated Output Offset

Calibration Procedure

The following procedure describes how to run calibration on all of the channels for every gain setting (after the devices are enabled and reset).

1. Enable each channel completely (i.e., power up the clocks, references, LDO, PGA, AAF, and so on).
2. Write the following register bits to the values shown, in the order shown:

- 0xA2 [5], 0xA9 [5], 0xB0 [5], 0xB7 [5] = 1 // Short the PGA inputs, reconfigure the AAF, and the enable comparator.
- 0x10 [7] = 1 // Enable the calibration engine clock
Although the enable bit does not self-clear, it is not necessary to clear the bit unless a new calibration is desired.
- 0x1E [3:0] = 0xF // Set the calibration clock frequency to 192kHz.
- 0x1E [4] = 1 // Apply the clock frequency change by transitioning bit 4 low to high.
- 0x12 [3:0] = 0xF // Enable each channel's digital calibration engine and start calibrating.

3. Wait for the calibration to complete for each channel by monitoring the following registers:

Channel 1 calibration status register 0xE3 [7:6], channel 2 calibration status register 0xE5 [7:6], channel 3 calibration status register 0xE7 [7:6], channel 4 calibration status register 0xE9 [7:6]

The calibration value is automatically used by the devices. Calibration results are 10-bit gain values stored in the following register locations:

- Channel 1 = 0xE3 [1:0] + 0xE2 [7:0]
- Channel 2 = 0xE5 [1:0] + 0xE4 [7:0]
- Channel 3 = 0xE7 [1:0] + 0xE6 [7:0]
- Channel 4 = 0xE9 [1:0] + 0xE8 [7:0]

(The uncalibrated code is defaulted to 0x200 (512 decimal, – 0 signed integer).)

A single-gain calibration is also possible by using the 0x13 ADC_OFFSET_CTRL1 register in place of step 2.

PGA Calibration Register Description

Table 39: ANA_ADC1_CTRL_3—0xA2

Bits	Name	Default	R/W	Description
5	RX1_ANA_CAL_EN	0	R/W	Place the Rx into calibration mode: 0 = Normal operation 1 = Shorts the PGA inputs, reconfigures the AAF, and enables the comparator

Registers 0xA9, 0xB0, and 0xB7 similarly control channels 2, 3, and 4, respectively.

Table 40: ADC_CLK_CTRL—0x10

Bits	Name	Default	R/W	Description
7	MIC_OFFSET_CLK_EN	0	R/W	Microphone offset calibration clock enable: 0 = Disables the clock for ADC offset calibration 1 = Enables the clock for ADC offset calibration

Table 41: MIC_OFFSET_CLK_CTRL—0x1E

Bits	Name	Default	R/W	Description
4	MIC_OFFSET_CLK_DIV [4]	0	R/W	Enable for the microphone offset calibration clock divisor change. When there is a 0-to-1 transition on this bit, the divisor value on mic_offset_clk_div[3:0] is latched.
3:0	MIC_OFFSET_CLK_DIV [3:0]	3	R/W	Divider control for the microphone offset calibration clock: $\text{offset_clock} = \text{source_clock} / (\text{mic_offset_clk_div}[3:0] + 1)$ The source clock can be SYS CLOCK/4. The default is 0x3 to achieve the 768kHz calibration clock.

Table 42: ADC_OFFSET_CTRL0—0x12

Bits	Name	Default	R/W	Description
3	MIC_OFFSET_CAL_EN4	0	R/W	Enables channel 4's SAR engine for one-time calibration: 0 = Disables the offset calibration engine 1 = Enables the calibration engine
2	MIC_OFFSET_CAL_EN3	0	R/W	Enables channel 3's SAR engine for one-time calibration: 0 = Disables the offset calibration engine 1 = Enables the calibration engine
1	MIC_OFFSET_CAL_EN2	0	R/W	Enables channel 2's SAR engine for one-time calibration: 0 = Disables the offset calibration engine 1 = Enables the calibration engine
0	MIC_OFFSET_CAL_EN1	0	R/W	Enables channel 1's SAR engine for one-time calibration: 0 = Disables the offset calibration engine 1 = Enables the calibration engine

Table 43: ADC_OFFSET_CTRL1—0x13

Bits	Name	Default	R/W	Description
7:3	MIC_OFFSET_CAL_GAIN [4:0]	0	R/W	The gain setting that the calibration is done for on the channel set by MIC_OFFSET_CAL_CHANNEL, if MIC_OFFSET_CALL_EN_SINGLE = 1.
2:1	MIC_OFFSET_CAL_CHANNEL	0	R/W	Selects the channel on which the particular gain set by MIC_OFFSET_CAL_GAIN[4:0] needs to be applied: • 0 = Channel 1 • 1 = Channel 2 • 2 = Channel 3 • 3 = Channel 4
0	MIC_OFFSET_CAL_EN_SINGLE	0	R/W	Enables the calibration for the single gain programmed by MIC_OFFSET_CAL_GAIN: • 0 = No calibration • 1 = Calibrate one-time for the programmed gain

Table 44: MIC1_OFFSET_LSB_STATUS—0xE2

Bits	Name	Default	R/W	Description
7:0	MIC1_OFFSET [7:0]	0	R	Channel 1 microphone path calibrated value that is sent to the analog. The 8-bit Least Significant Bit (LSB) of 10-bit value is read here.

Table 45: MIC1_OFFSET_MSB_STATUS—0xE3

Bits	Name	Default	R/W	Description
7	MIC1_OFFSET_CAL_DONE	0	R	Status that indicates if the calibration is complete: • 0 = One-time calibration did not complete • 1 = One-time calibration is complete
6	MIC1_OFFSET_CAL_RUN_STATUS	0	R	Describes whether the microphone offset calibration engine is still calibrating: • 0 = Calibration is inactive • 1 = Calibration is in process
5:2	Reserved	0	R	-
1:0	MIC1_OFFSET [9:8]	2	R	Channel 1 microphone path calibrated value that is sent to the analog. The 2-bit LSB of the 10-bit value is read here. The default is 10-bit value = 200 (hex) = 512 (dec) = –0 (sign mag).

Registers 0xE4 through 0xE9 similarly provide status for channels 2, 3, and 4, respectively.

Performance Data

Table 46: PGA Specifications

Parameter	Minimum	Typical	Maximum	Units
Temperature	−40	27	125	°C
Supply Voltage—VDD33_ANA_x	2.7	3.1	3.6	V
Input Resistance	-		-	kΩ
Gain = −6dB		16		
Gain = 0dB		5		
Gain = 3dB–30dB (programmable)		500, 250, 125, 25		
Gain Step	-	1	-	dB
Uncalibrated Output Offset	-	-	-	mV
Calibrated Offset	-	-	1	mV
THD (1kHz tone, −1dBFS)	-		-	dB
Gain = −6dB		−115		
Gain = 0dB		−96.1		
Gain = 6dB		−95.4		
Gain = 12dB		−93.5		
Gain = 24dB		−90.8		
Input Referred Noise (20Hz–20kHz)	-			dBV
Gain = −6dB		−105.1	-	
Gain = 0dB		−108.9	-	
Gain = 6dB		−116.8	114.1	
Gain = 12dB		−119.9	116.6	
Gain = 24dB		−122.4	118.6	
SNR (20Hz–20kHz)			-	dBV
Gain = −6dB	-	111.1		
Gain = 0dB	-	108.9		
Gain = 6dB	108.1	110.9		
Gain = 12dB	104.5	107.8		
Gain = 24dB	94.4	98.3		
Pop at Mute/unmute	-	-	−65	dBV A-w
Pop at Minimum Gain Change	-	-	−50	
Quiescent Current	-		-	mA
Gain = −6dB/0dB		0.27		
Gain = 3dB–30dB		1.19		

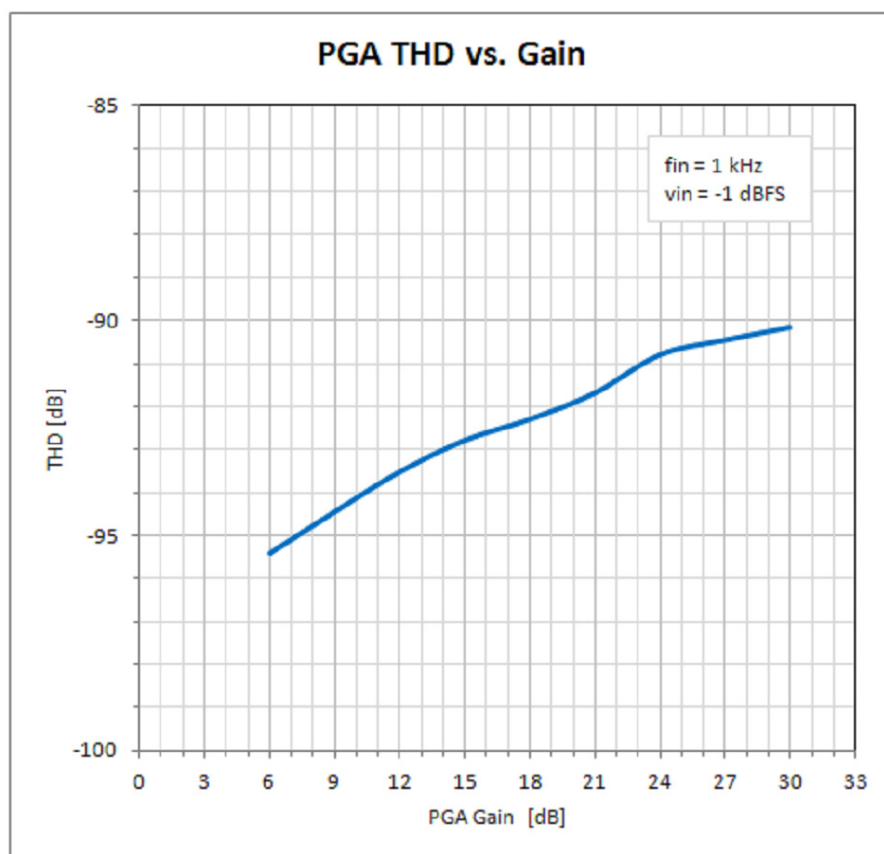


Figure 50: PGA THD vs Gain

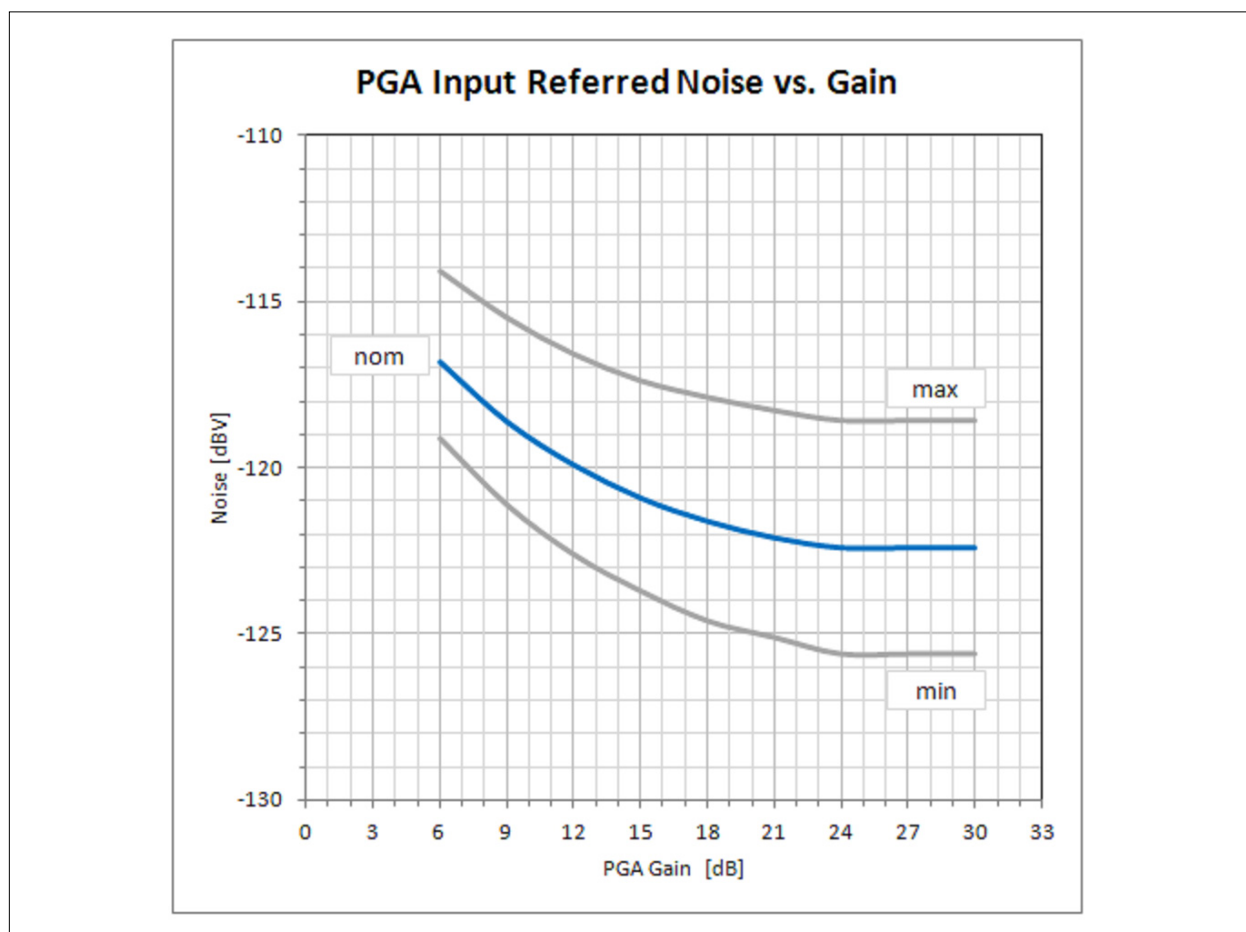


Figure 51: PGA Input Noise Performance

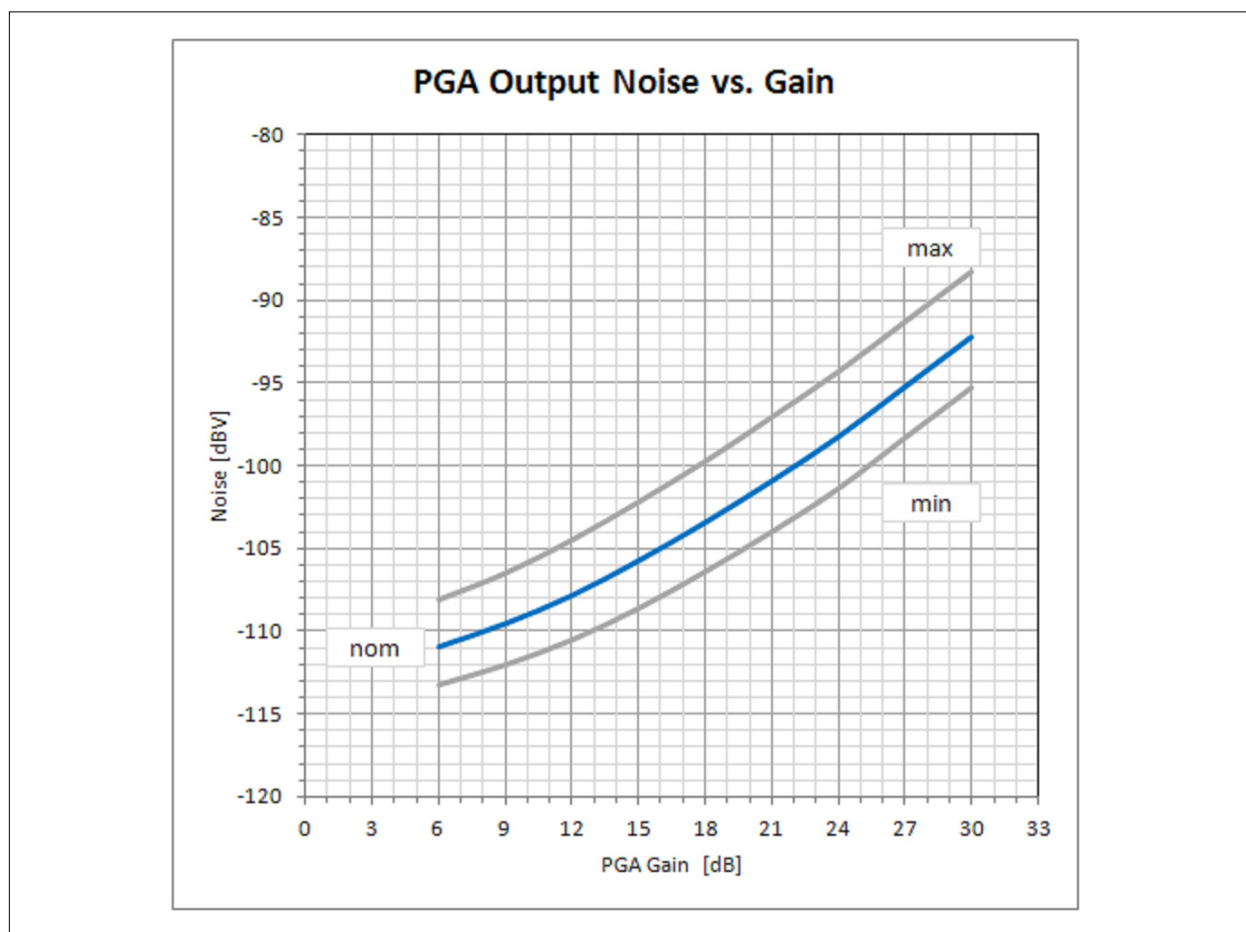


Figure 52: PGA Output Noise Performance

Anti-Aliasing Filter (AAF)

Block Diagram

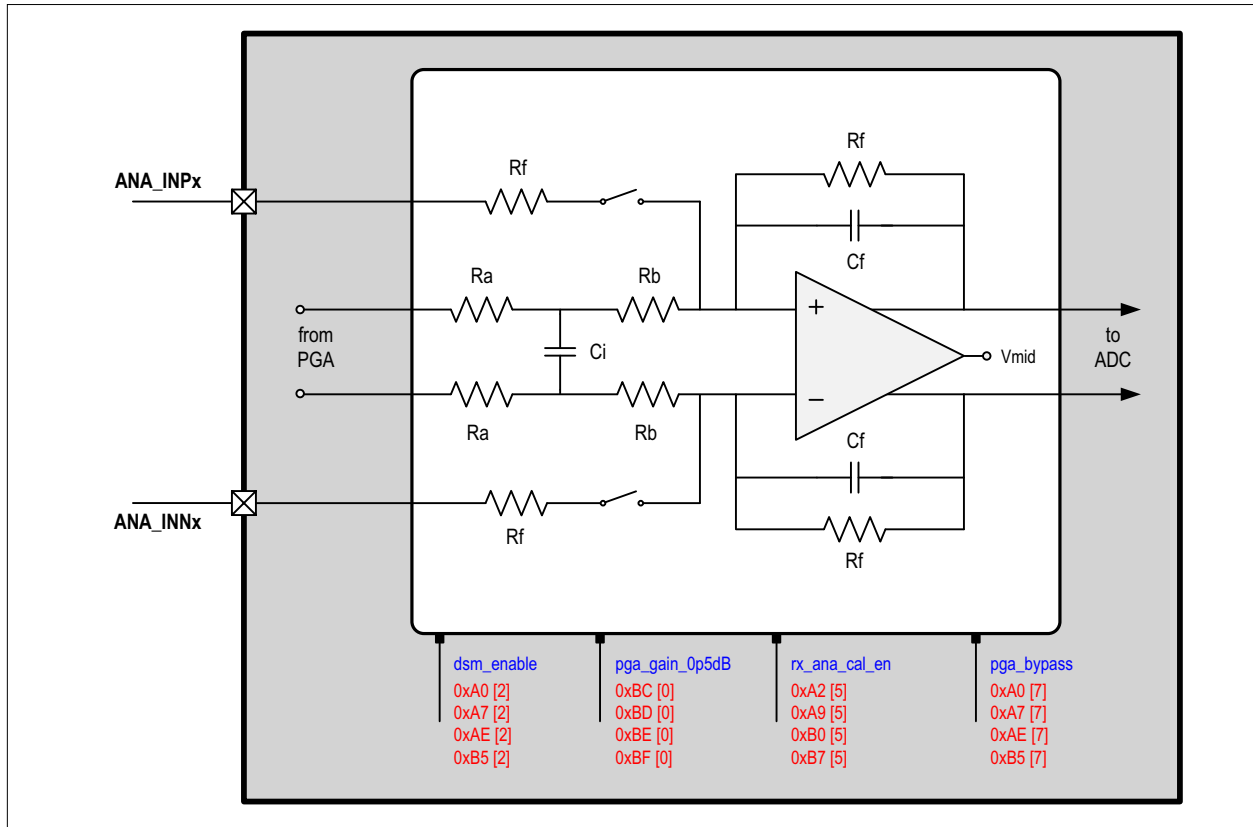


Figure 53: AAF Block Diagram

Block Description

The ADC block consists of an anti-aliasing lowpass filter (AAF) and a multi-bit, over-sampling delta-sigma modulator (DSM). The AAF low pass filters the PGA's $2V_{RMS}$ output signal with a set low frequency attenuation; the attenuation is required to ensure stable DSM operation. The AAF's corner filter of 1 MHz is combined with the external lowpass filtering and PGA filtering to ensure at least ~60 dB attenuation at the modulator switching frequency of approximately 12 MHz. This filtering is required to minimize the noise that will be folded down to the audio band by the oversampling ADC. See ["External Input Configurations"](#) on page 88 for notes on selecting external component values.

The normalized low-pass transfer function of the entire chain (from the MIC to ADC input), including the external filtering, PGA, and AAF is approximately:

$$H(s) = \frac{1}{(1 + s \cdot \tau_1)(1 + s \cdot \tau_2)(1 + s \cdot \tau_3)(1 + s \cdot \tau_4)}$$

$$\text{where } \tau_1 = R_{source} C_{AAF}, \tau_2 = 72.1 \text{ ns}, \tau_3 = 51.2 \text{ ns}, \& \tau_4 = 108.7 \text{ ns},$$

Using this equation, an appropriate external C_{AAF} and total R_{SOURCE} can be selected to achieve at least 60 dB of attenuation at the ADC's switching frequency. For example, the attenuation at 12 MHz solely due to τ_2 , τ_3 and τ_4 is 45 dB. In order for τ_1 to contribute an additional 15 dB of attenuation at 12 MHz, the corner frequency of the external filtering must be approximately 2.6 MHz, or $\tau_1 = R_{SOURCE} C_{AAF} = 61 \text{ ns}$.

In addition to its normal filtering operation, the AAF includes the following auxiliary functionalities:

- The PGA implements a 0.5 dB gain boost (see 0xBC [0]) that works with the PGA gain control to achieve an effective 0.5 dB programming increment
- When the receiver is set up for offset calibration (see 0xA2 [5]), the AAF is reconfigured into a high gain pre-amplifier for the subsequent comparator.
- For high performance line input applications, the PGA can be bypassed (see 0xA0 [7]) and the channel inputs can be routed directly into the AAF inputs with 0 dB gain.

Register Description

Table 47: ANA_ADC1_CTRL_1—0xA0

Bits	Name	Default	R/W	Description
7	RX1_PGA_BYPASS	0	R/W	Channel 1 PGA bypass for the line-in mode: 0 = Does not bypass the PGA path 1 = Bypasses the PGA and routes the inputs directly into the AAF with 0dB gain
2	RX1_DSM_ENABLE	0	R/W	Enables the channel 1 AAF and ADC: 0 = Shuts down the AAF and ADC 1 = Enables the AAF and ADC

Registers 0xA7, 0xAE, and 0xB5 similarly control channels 2, 3, and 4, respectively.

Table 48: ANA_ADC1_CTRL_3—0xA2

Bits	Name	Default	R/W	Description
5	RX1_ANA_CAL_EN	0	R/W	Place the Rx into calibration mode: 0 = Normal operation 1 = Shorts the PGA inputs, reconfigures the AAF, and enables the comparator

Registers 0xA9, 0xB0, and 0xB7 similarly control channels 2, 3, and 4, respectively.

Table 49: ADC1_ANALOG_PGA_GAIN—0xBC

Bits	Name	Default	R/W	Description
0	RX1_ANALOG_PGA [0]	0	R/W	Channel 1 PGA 0.5dB step (implemented in AAF): 0 = 0.0dB 1 = 0.5dB

Registers 0xBD, 0xBE, and 0xBF similarly control channels 2, 3, and 4, respectively.

Performance Data

Table 50: AAF Specifications

Parameter	Minimum	Typical	Maximum	Units
Temperature	−40	27	125	°C
Supply Voltage—VDD33_ANA_x	2.7	3.1	3.6	V
Attenuation @ 12.388MHz				dB
AAF Only	-	32	-	
With PGA	-	46	-	
With PGA and External Filtering	60	70	-	
In-band droop		0.44		dB
Output Referred Noise (PGA + AAF)	-			dBV
In-band = 20Hz–20kHz		−109.9	−108.2	
Out-of-band = Up to 200MHz		−115.3	−114.9	
Out-of-band = Up to 1GHz		−113.3	−113.1	
THD (1kHz tone, −1dBFS)	-	−90	-	dB
Current Consumption	-	4.2	-	mA

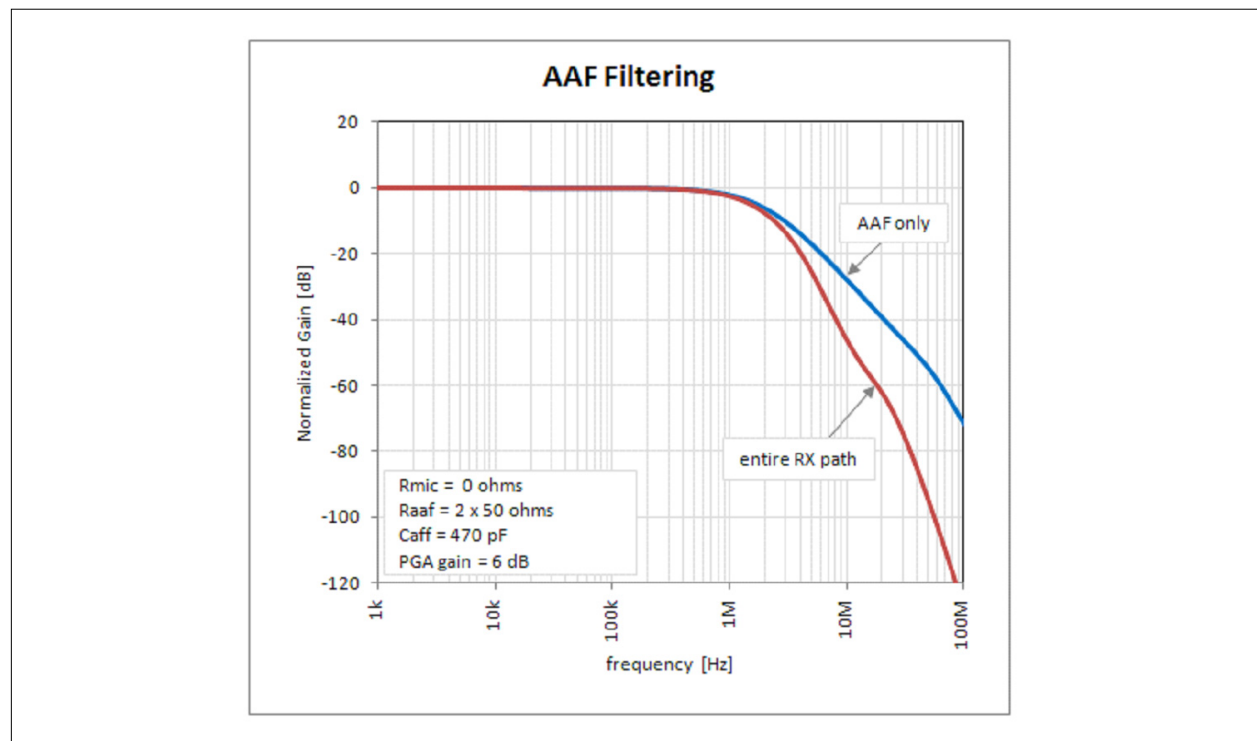


Figure 54: AAF

Analog-to-Digital Converter (ADC)

Block Description

The ADC implementation in the CX20810/CX20811 is a multi-bit, over-sampling DSM. The digital output of the DSM is then decimated down to the required sample rate and the DC cancellation, additional filtering, and digital amplification are implemented. Finally, a digital selector and mixer is available to map any analog input into any channel, or combine multiple channels into a high performance single channel.

All the ADCs in the devices share the same sample clock (i.e., all the sample rates are the same). Each ADC has an independent digital PGA with a gain of -74dB to 12dB , with 0.125dB gain resolution. There is a gain ramping mechanism that ramps up/down the gain based on the selected gain step, selected from 0.25dB , 0.5dB , or 1dB . The gain change rate occurs at the F_s sample rate by default. Each ADC has an available digital DC filter to remove offsets from the analog.

Within the converter, there is a channel selector that allows each channel to select any one of the four signals coming from the analog.

Example: Channel 0 can be configured to select the signal from analog input 3.

Pin Description

For definitions of the I/O Type acronyms used in the following table, see "Signal Definitions" on page 34.

Table 51: Analog VC Pin Description

Pin Label	Pin Number			I/O Type	Signal Name/Description
	CX20810-11Z	CX20811-11Z	CX20811-15Z		
ANA_INP1	22	30	G2	Ia	ADC1 Positive Input. Positive microphone input signal for channel 1.
ANA_INN1	23	31	F2	Ia	ADC1 Negative Input. Negative/GND-sense microphone input signal for channel 1.
ANA_INP2	25	33	H1	Ia	ADC2 Positive Input. Positive microphone input signal for channel 2.
ANA_INN2	26	34	G1	Ia	ADC2 Negative Input. Negative/GND-sense microphone input signal for channel 2.
ANA_INP3	35	44	A1	Ia	ADC3 Positive Input. Positive microphone input signal for channel 3.
ANA_INN3	36	45	B1	Ia	ADC3 Negative Input. Negative/GND-sense microphone input signal for channel 3.
ANA_INP4	38	47	B3	Ia	ADC4 Positive Input. Positive microphone input signal for channel 4.
ANA_INN4	39	48	A2	Ia	ADC4 Negative Input. Negative/GND-sense microphone input signal for channel 4.

ADC Decimation Chain

The decimation chain receives a multi-bit stream at 12.288MHz or 6.144MHz from the DSM in the analog domain, and down-samples to the required sample rate application needs.

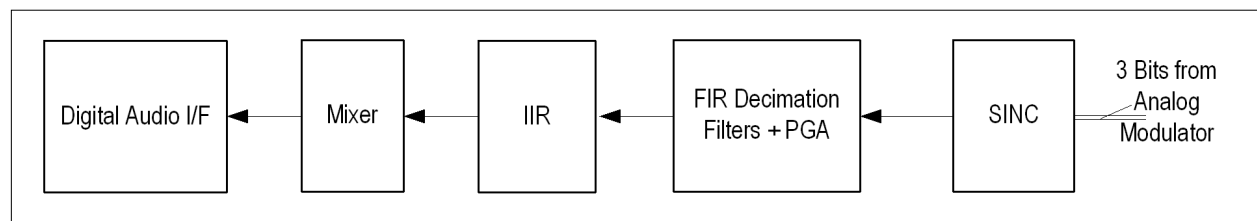


Figure 55: Decimation Chain

Features

- Supports sample rates of:
 - 8kHz
 - 16kHz
 - 24kHz
 - 32kHz
 - 44.1kHz
 - 48kHz
 - 96kHz
- Independent clock gating enables are available for each of the ADC's channels
- Sample rates of each ADC are shared (i.e., all ADCs work on the same sample rate as the requirement)
- Independent PGA (–74dB to 12dB) on each channel that has a step resolution of 0.125dB.
- Infinite Impulse Response (IIR) filters
- Mixer
- 24-bit data interface routes the signal to the I²S

Decimation

A DSP system with an analog audio input signal in the range 0kHz to 20kHz uses down-sampling techniques to convert the analog multi-bit/single stream at a high rate to a 2's complement digital code at a low rate. The design supports the four-channel ADC. The decimation chain consists of:

- SINC filter
- Finite Impulse Response (FIR) filter chain

Gain

- Gain 1.66dB = Because the digital chain compensates for the –1.159dB signal mapping loss plus the modulator loss of 0.5dB, plus the gain loss in the analog, the total gain compensated is $(1.159 + 0.5) \approx 1.66\text{dB}$. When the signal is selected from the analog modulator, it goes through a gain stage. There is a bypass option for this fixed gain compensation.
- Gain stage (–74dB to 12dB) = The PGA has a step resolution of 0.125dB, and a Read-Only Memory (ROM) table mechanism is used for the PGA calculation. The coefficients in the ROM table are created and stored as hard-coded values. The ROM table contains the coefficients for the gain stage from –74dB to 12dB, with steps of 0.125dB

Although the gain ramping can be programmable in 1dB, 0.5dB, or 0.25dB based on the control bits, by default it works in 0.125dB steps.

Mute

There are 2 mute functions available in the ADC data path:

- Hard mute = When set as defined by register 0x18, the ADC output forces to 0 from any signal value.
- Soft mute = Defined in the PGA registers (0x20 to 0x27), this can be achieved by programming the PGA register to 0. In this case, the value ramps smoothly depending on the ramping step and ramping step time (defined in register 0x1A). The signal ramps from the signal level when the PGA is applied to mute (value of 0).

The ramping time depends on the programmed ramping step (0x20 to 0x28) and step time (0x1A). The worst-case ramping time can be calculated from the maximum programmed PGA value of 0x2B8 to 0x0 in steps of 1, 2, 4, or 8 at F_s , $F_s/2$, $F_s/4$, or $4 * F_s$ steps.

Mixer

The mixer block sums the channels from the MIC before feeding to the selected decimator block of the digital ADC chain. The following lists the possible options:

- Sum of the left channels of two stereo MICs
- Sum of the right channels of two stereo MICs
- Sum of the left and right channels of a stereo MIC1
- Sum of the left and right channels of a stereo MIC2
- Sum of all the channels

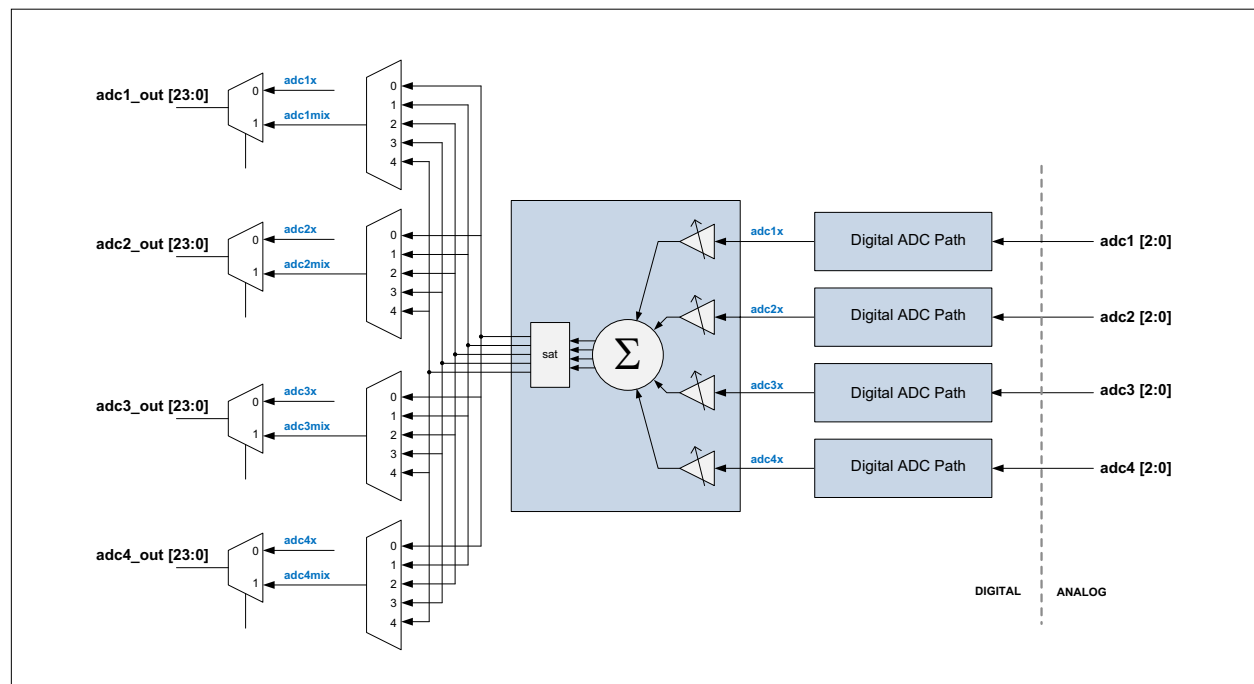


Figure 56: Mixer Block

The mixer has its own small PGA that can be applied on all the inputs, and ranges from 2dB to -30dB as described in registers 0x1B and 0x1C.

Register Description

ADC_CLK_CTRL—0x10

Table 52: ADC_CLK_CTRL—0x10

Bits	Name	Default	R/W	Description
7	MIC_OFFSET_CLK_EN	0	R/W	Microphone offset calibration clock enable: 0 = Disables the clock for ADC offset calibration 1 = Enables the clock for ADC offset calibration
6	ADC_CLK_GATE_EN	0	R/W	Analog microphone clock gate enable: 0 = Disables the analog clock for the ADC channel 1 = Enables the analog clock to the ADC channel
5	ADC_CLK_SELECT	0	R/W	Analog microphone clock select: 0 = Sets the analog microphone clock to 12.288MHz 1 = Sets the analog microphone clock to 6.144MHz
4	ADC_CLK_CH4_EN	0	R/W	Clock gate enable for ADC4: 0 = Disables the clock to ADC channel 4 1 = Enables the clock to ADC channel 4
3	ADC_CLK_CH3_EN	0	R/W	Clock gate enable for ADC3: 0 = Disables the clock to ADC channel 3 1 = Enables the clock to ADC channel 3
2	ADC_CLK_CH2_EN	0	R/W	Clock gate enable for ADC2: 0 = Disables the clock to ADC channel 2 1 = Enables the clock to ADC channel 2
1	ADC_CLK_CH1_EN	0	R/W	Clock gate enable for ADC1: 0 = Disables the clock to ADC channel 1 1 = Enables the clock to ADC channel 1
0	ADC_CLK_ALL_EN	0	R/W	Clock gate enable for ADC digital: 0 = Disables the clock to all ADC channels 1 = Enables the clock to all ADC channels

ADC_EN_CTRL—0x11**Table 53: ADC_EN_CTRL—0x11**

Bits	Name	Default	R/W	Description
7	MIXER EN	0	R/W	When set, enables the mixer block based on how the ADC mapping mixer output is routed: 0 = Disables the mixer 1 = Enables the mixer
6:4	ADC_SAMPLE_RATE[2:0]	1	R/W	Sets the sample rate for all ADC channels: 0 = 8kHz 1 = 16kHz 2 = 24kHz/22.05kHz, based on the PLL or external MCLK 3 = 32kHz 4 = 48kHz/44.1kHz, based on the PLL or external MCLK 5 = 96kHz/88.2kHz based on the PLL or external MCLK 6 = Reserved 7 = Reserved
3	ADC_EN_CTRL[3]	0	R/W	Enable for ADC4: 0 = Disables ADC channel 4 1 = Enables ADC channel 4
2	ADC_EN_CTRL[2]	0	R/W	Enable for ADC3: - Disables ADC channel 3 - Enables ADC channel 3
1	ADC_EN_CTRL[1]	0	R/W	Enable for ADC2: - Disables ADC channel 2 - Enables ADC channel 2
0	ADC_EN_CTRL[0]	0	R/W	Enable for ADC1: - Disables ADC channel 1 - Enables ADC channel 1

MIXER_CTRL_0—0x14**Table 54: MIXER_CTRL_0—0x14**

Bits	Name	Default	R/W	Description
7:5	MIXER_CTRL0 [7:5]	0	R/W	Selects the mixer mode for ADC2: • 000 = Sum of the left channels (adc1+adc3) • 001 = Sum of the right channels (adc2+adc4) • 010 = Sum of the left and right channels (adc1+adc2) • 011 = Sum of the left and right channels (adc3+adc4) • 100 = Sum of all channels
4:2	MIXER_CTRL0 [4:2]	0	R/W	Selects the mixer mode for ADC1: • 000 = Sum of the left channels (adc1+adc3) • 001 = Sum of the right channels (adc2+adc4) • 010 = Sum of the left and right channels (adc1+adc2) • 011 = Sum of the left and right channels (adc3+adc4) • 100 = Sum of all channels
1	MIXER_CTRL0 [1]	0	R/W	Selects the mixer output on the ADC2 channel: • 0 = No operation (the mixer block, even if enabled, does not interfere in the normal microphone path) • 1 = Mixer output on ADC2
0	MIXER_CTRL0 [0]	0	R/W	Selects the mixer output on the ADC1 channel: • 0 = No operation (the mixer block, even if enabled, does not interfere in the normal microphone path) • 1 = Mixer output on ADC1

MIXER_CTRL_1—0x15**Table 55: MIXER_CTRL_1—0x15**

Bits	Name	Default	R/W	Description
7:5	MIXER_CTRL1 [7:5]	0	R/W	Selects the mixer mode for ADC4: • 000 = Sum of the left channels (adc1+adc3) • 001 = Sum of the right channels (adc2+adc4) • 010 = Sum of the left and right channels (adc1+adc2) • 011 = Sum of the left and right channels (adc3+adc4) • 100 = Sum of all channels
4:2	MIXER_CTRL1 [4:2]	0	R/W	Selects the mixer mode for ADC3: • 000 = Sum of the left channels (adc1+adc3) • 001 = Sum of the right channels (adc2+adc4) • 010 = Sum of the left and right channels (adc1+adc2) • 011 = Sum of the left and right channels (adc3+adc4) • 100 = Sum of all channels
1	MIXER_CTRL1 [1]	0	R/W	Selects the mixer output on ADC4 channel: • 0 = No operation (the mixer block, even if enabled, does not interfere in the normal microphone path) • 1 = Mixer output on ADC4
0	MIXER_CTRL1 [0]	0	R/W	Selects the mixer output on ADC3 channel: • 0 = No operation (the mixer block, even if enabled, does not interfere in the normal microphone path) • 1 = Mixer output on ADC3

ADC_MAP_CTRL1—0x17**Table 56: ADC_MAP_CTRL1—0x17**

Bits	Name	Default	R/W	Description
7:6	ADC_MAP_CTRL1 [7:6]	0	R/W	Maps that the analog microphone input is connected to for digital ADC4: • 00 = Analog Mic4 • 01 = Analog Mic1 • 10 = Analog Mic2 • 11 = Analog Mic3
5:4	ADC_MAP_CTRL1 [5:4]	0	R/W	Maps that the analog microphone input is connected to for digital ADC3: • 00 = Analog Mic3 • 01 = Analog Mic4 • 10 = Analog Mic1 • 11 = Analog Mic2
3:2	ADC_MAP_CTRL1 [3:2]	0	R/W	Maps that the analog microphone input is connected to for digital ADC2: • 00 = Analog Mic2 • 01 = Analog Mic3 • 10 = Analog Mic4 • 11 = Analog Mic1
1:0	ADC_MAP_CTRL1 [1:0]	0	R/W	Maps that the analog microphone input is connected to for digital ADC1: • 00 = Analog Mic1 • 01 = Analog Mic2 • 10 = Analog Mic3 • 11 = Analog Mic4

MIXER0_PGA—0x1B**Table 57: MIXER0_PGA—0x1B**

Bits	Name	Default	R/W	Description
7	MIXER0_PGA_1[3]	0	R/W	Mixer mute for ADC channel 2: 1 = Mutes the mixer input from ADC channel 2 0 = No mute
6:4	MIXER0_PGA_1[2:0]	1	R/W	Mixer PGA for ADC channel 2. The gain on the input data from the ADC2 channel: 000 = 2dB 001 = 0dB 010 = -2.5dB 011 = -6dB 100 = -12dB 101 = -18dB 110 = -24dB 111 = -30dB
3	MIXER0_PGA_0[3]	0	R/W	Mixer mute for ADC channel 1: 1 = Mutes the mixer input from ADC channel 1 0 = No mute
2:0	MIXER0_PGA_0[2:0]	1	R/W	Mixer PGA for ADC channel 1. The gain on the input data from the ADC1 channel: 000 = 2dB 001 = 0dB 010 = -2.5dB 011 = -6dB 100 = -12dB 101 = -18dB 110 = -24dB 111 = -30dB

MIXER1_PGA—0x1C**Table 58: MIXER1_PGA—0x1C**

Bits	Name	Default	R/W	Description
7	MIXER1_PGA_1[3]	0	R/W	Mixer mute for ADC channel 4: 1 = Mutes the mixer input from ADC channel 4 0 = No mute
6:4	MIXER1_PGA_1[2:0]	1	R/W	Mixer PGA for ADC channel 4. The gain on the input data from the ADC4 channel: 000 = 2dB 001 = 0dB 010 = -2.5dB 011 = -6dB 100 = -12dB 101 = -18dB 110 = -24dB 111 = -30dB
3	MIXER1_PGA_0[3]	0	R/W	Mixer mute for ADC channel 3: 1 = Mutes the mixer input from ADC channel 3 0 = No mute
2:0	MIXER1_PGA_0[2:0]	1	R/W	Mixer PGA for ADC channel 3. The gain on the input data from the ADC3 channel: 000 = 2dB 001 = 0dB 010 = -2.5dB 011 = -6dB 100 = -12dB 101 = -18dB 110 = -24dB 111 = -30dB

DSP_CLK_CTRL—0x1D**Table 59: DSP_CLK_CTRL—0x1D**

Bits	Name	Default	R/W	Description
7:4	Reserved	0	-	Reserved.
3	DSP_CLK_CTRL [3]	0	R/W	Clock gate enable for the IIR biquad on ADC4: 0 = Disables the clock to the IIR biquad 1 = Enables the clock to the IIR biquad
2	DSP_CLK_CTRL [2]	0	R/W	Clock gate enable for the IIR biquad on ADC3: 0 = Disables the clock to the IIR biquad 1 = Enables the clock to the IIR biquad
1	DSP_CLK_CTRL [1]	0	R/W	Clock gate enable for the IIR biquad on ADC2: 0 = Disables the clock to the IIR biquad 1 = Enables the clock to the IIR biquad
0	DSP_CLK_CTRL [0]	0	R/W	Clock gate enable for the IIR biquad on ADC1: 0 = Disables the clock to the IIR biquad 1 = Enables the clock to the IIR biquad

ADC1_PGA_LSB—0x20**Table 60: ADC1_PGA_LSB—0x20**

Bits	Name	Default	R/W	Description
7:0	ADC1_PGA_LSB [7:0]	0x58	R/W	Sets the digital PGA for the ADC1 channel. Program this LSB register first, followed by the MSB register for the gain value to be effective. See Table 61 for details.

ADC1_PGA_MSB—0x21**Table 61: ADC1_PGA_MSB—0x21**

Bits	Name	Default	R/W	Description
7:4	Reserved	0	-	Reserved.
3:2	ADC1_PGA_MSB [3:2]	0	R/W	Controls the ramping steps for the ADC1 digital PGA: 00 = Steps at $\pm 0.125\text{dB}$ 01 = Steps at $\pm 0.25\text{dB}$ 10 = Steps at $\pm 0.5\text{dB}$ 11 = Steps at $\pm 1\text{dB}$
1:0	ADC1_PGA_MSB [9:8]	0x2	R/W	Sets the digital PGA for the ADC1 channel. Program the LSB register first, followed by this MSB register for the gain value to be effective. The gain is calculated by: $[(-75) + ((0.125) * (\text{decimal value of ADC1_PGA_MSB:LSB}))]$ Example: - To set 0dB gain with 0.125dB steps, write: 0x58 to ADC1_PGA_LSB[7:0] 0x02 to ADC1_PGA_MSB[9:8] - To set -20dB gain with 0.125dB steps, write: 0xB8 to ADC1_PGA_LSB[7:0] 0x01 to ADC1_PGA_MSB[9:8]

ADC2_PGA_LSB—0x22**Table 62: ADC2_PGA_LSB—0x22**

Bits	Name	Default	R/W	Description
7:0	ADC2_PGA_LSB [7:0]	0x58	R/W	Sets the digital PGA for the ADC2 channel. Program this LSB register first, followed by the MSB register for the gain value to be effective. See Table 63 for details.

ADC2_PGA_MSB—0x23**Table 63: ADC2_PGA_MSB—0x23**

Bits	Name	Default	R/W	Description
7:4	Reserved	0	-	Reserved.
3:2	ADC2_PGA_MSB [3:2]	0	R/W	Controls the ramping steps for the ADC2 digital PGA: • 00 = Steps at $\pm 0.125\text{dB}$ • 01 = Steps at $\pm 0.25\text{dB}$ • 10 = Steps at $\pm 0.5\text{dB}$ • 11 = Steps at $\pm 1\text{dB}$
1:0	ADC2_PGA_MSB [8]	0x2	R/W	Sets the digital PGA for the ADC2 channel. Program the LSB register first, followed by this MSB register for the gain value to be effective. The gain is calculated by: $[(-75) + ((0.125) * (\text{decimal value of ADC2_PGA_MSB:LSB}))]$ Example: – To set 0dB gain with 0.125dB steps, write: • 0x58 to ADC2_PGA_LSB[7:0] • 0x02 to ADC2_PGA_MSB[9:8] – To set –20dB gain with 0.125dB steps, write: • 0xB8 to ADC2_PGA_LSB[7:0] • 0x01 to ADC2_PGA_MSB[9:8]

ADC3_PGA_LSB—0x24**Table 64: ADC3_PGA_LSB—0x24**

Bits	Name	Default	R/W	Description
7:0	ADC3_PGA_LSB [7:0]	0x58	R/W	Sets the digital PGA for the ADC3 channel. Program this LSB register first, followed by the MSB register for the gain value to be effective. See Table 65 for details.

ADC3_PGA_MSB—0x25**Table 65: ADC3_PGA_MSB—0x25**

Bits	Name	Default	R/W	Description
7:4	Reserved	0	R/W	Reserved.
3:2	ADC3_PGA_MSB [3:2]	0	R/W	Controls the ramping steps for the ADC3 digital PGA: • 00 = Steps at ± 0.125dB • 01 = Steps at ± 0.25dB • 10 = Steps at ± 0.5dB • 11 = Steps at ± 1dB
1:0	ADC3_PGA_MSB [9:8]	0x2	R/W	Sets the digital PGA for the ADC3 channel. Program the LSB register first, followed by this MSB register for the gain value to be effective. The gain is calculated by: $[(-75) + ((0.125) * (\text{decimal value of ADC3_PGA_MSB:LSB}))]$ Example: – To set 0dB gain with 0.125dB steps, write: • 0x58 to ADC3_PGA_LSB[7:0] • 0x02 to ADC3_PGA_MSB[9:8] – To set –20dB gain with 0.125dB steps, write: • 0xB8 to ADC3_PGA_LSB[7:0] • 0x01 to ADC3_PGA_MSB[9:8]

ADC4_PGA_LSB—0x26**Table 66: ADC4_PGA_LSB—0x26**

Bits	Name	Default	R/W	Description
7:0	ADC4_PGA_LSB [7:0]	0x58	R/W	Sets the digital PGA for the ADC4 channel. Program this LSB register first, followed by the MSB register for the gain value to be effective. See Table 67 for details.

ADC4_PGA_MSB—0x27**Table 67: ADC4_PGA_MSB—0x27**

Bits	Name	Default	R/W	Description
7:4	Reserved	0	-	Reserved.
3:2	ADC4_PGA_MSB [3:2]	0	R/W	Controls the ramping steps for the ADC4 digital PGA: • 00 = Steps at ±0.125dB • 01 = Steps at ±0.25dB • 10 = Steps at ±0.5dB • 11 = Steps at ±1dB
1:0	ADC4_PGA_MSB [9:8]	0x2	R/W	Sets the digital PGA for the ADC4 channel. Program the LSB register first, followed by this MSB register for the gain value to be effective. The gain is calculated by: $[(-75) + ((0.125) * (\text{decimal value of ADC4_PGA_MSB:LSB}))]$ Example: – To set 0dB gain with 0.125dB steps, write: • 0x58 to ADC4_PGA_LSB[7:0] • 0x02 to ADC4_PGA_MSB[9:8] – To set –20dB gain with 0.125dB steps, write: • 0xB8 to ADC4_PGA_LSB[7:0] • 0x01 to ADC4_PGA_MSB[9:8]

Infinite Impulse Response (IIR)

The CX20810/CX20811 supports four biquad IIRs in the ADC path with coefficients that are programmable to get the desired frequency response.

Block Diagram

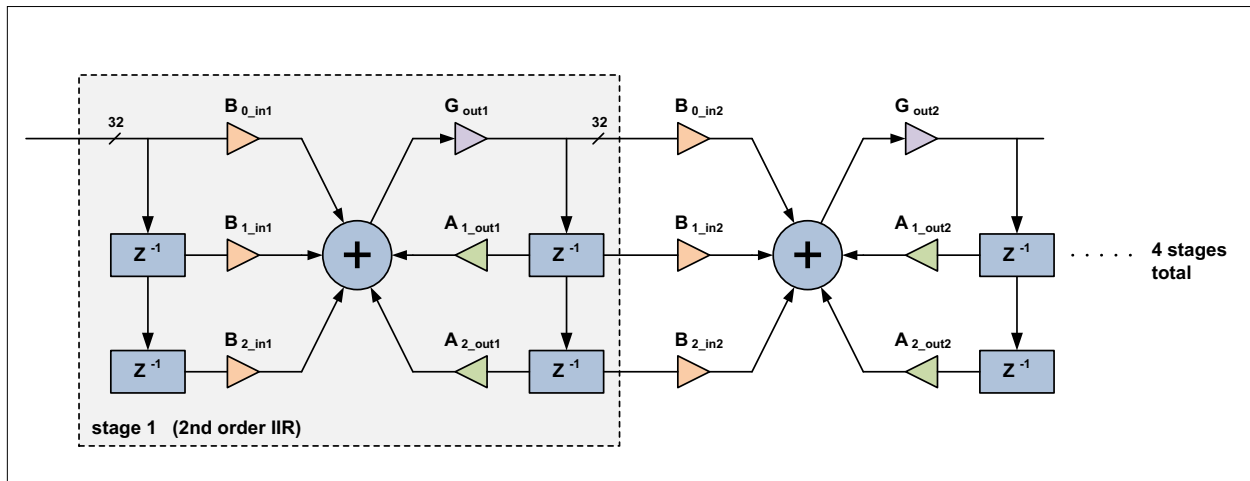


Figure 57: IIR Block Diagram

The implementation consists of four, second-order IIRs in series within each channel. Each second-order IIR has three forward coefficients of B_0 , B_1 , and B_2 that operate on the input, two feedback coefficients of A_1 and A_2 that operate on the output, and a scaling factor G .

The IIR can be described with the transfer function:

$$H(Z) = GB_0 + GB_1 Z^{-1} + GB_2 Z^{-2} / 1 - GA_1 Z^{-1} - GA_2 Z^{-2}$$

And the output is expressed as:

$$Y_n = G (A_1 Y_{n-1} + A_2 Y_{n-2} + B_0 X_n + B_1 X_{n-1} + B_2 X_{n-2})$$

Because the coefficients are programmable, there is full flexibility of the filter type, band frequency, Quality (Q) factor, and gain. The only limitation, which results from the fixed point resolution of 16 bits per coefficient, is that the band's frequency usually cannot be below 60Hz (at a 48kHz sampling rate).

Programming of Equalizer (EQ) Coefficients

The IIR block must be enabled to load coefficients from the control interface. The set of coefficients for the IIR needs to be loaded and the COEFF_IIR needs to be set first before enabling COEFF_LATCH_EN from the control interface. When the coefficient latch enable is set, the coefficients are stored in a 32-bit format by appending two 16-bit coefficients.

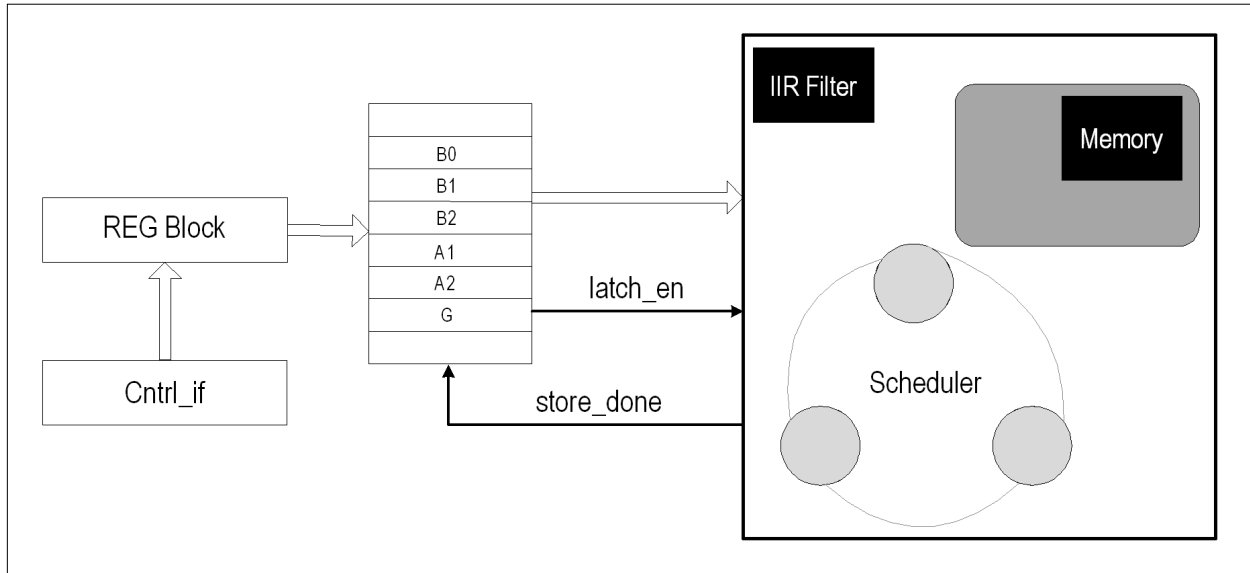


Figure 58: Coefficient Write from Control Interface to IIR

After the enable and reset release, all the memory is initialized with zeros and coefficients are written when LATCH_EN is set. The B0, B1, B2, A1, A2, and G coefficients are written to a Random Access Memory (RAM) location based on the channel selected (COEFF_CH) and IIR stage programmed (COEFF_IIR). When the coefficients are written to the 7x16 register table, the COEFF_LATCH_EN signal should be set high and the IIR detects a rising edge in COEFF_LATCH_EN and starts the transfer to the RAM. When the process is done, the IIR sets STORE_DONE high, which automatically clears COEFF_LATCH_EN when read from the control interface.

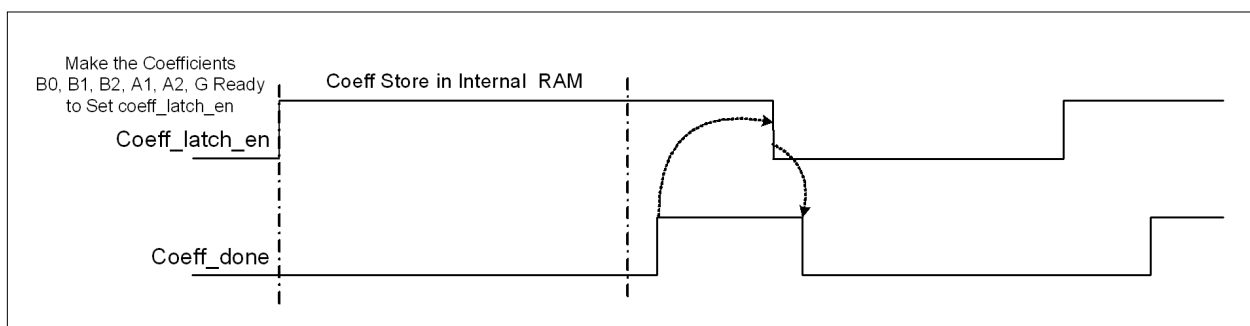


Figure 59: IIR Coefficient Programming

Register Description

IIR_COEFF_B0_LOW—0x90

Table 68: IIR_COEFF_B0_LOW—0x90

Bits	Name	Default	R/W	Description
7:0	B0[7:0]	0x00	R/W	IIR coefficient B0 lower byte.

IIR_COEFF_B0_HIGH—0x91

Table 69: IIR_COEFF_B0_HIGH—0x91

Bits	Name	Default	R/W	Description
7:0	B0[15:8]	0x00	R/W	IIR coefficient B0 higher byte.

IIR_COEFF_B1_LOW—0x92

Table 70: IIR_COEFF_B1_LOW—0x92

Bits	Name	Default	R/W	Description
7:0	B1[7:0]	0x00	R/W	IIR coefficient B1 lower byte.

IIR_COEFF_B1_HIGH—0x93

Table 71: IIR_COEFF_B1_HIGH—0x93

Bits	Name	Default	R/W	Description
7:0	B1[15:8]	0x00	R/W	IIR coefficient B1 higher byte.

IIR_COEFF_B2_LOW—0x94

Table 72: IIR_COEFF_B2_LOW—0x94

Bits	Name	Default	R/W	Description
7:0	B2[7:0]	0x00	R/W	IIR coefficient B2 lower byte.

IIR_COEFF_B2_HIGH—0x95

Table 73: IIR_COEFF_B2_HIGH—0x95

Bits	Name	Default	R/W	Description
7:0	B2[15:8]	0x00	R/W	IIR coefficient B2 higher byte.

IIR_COEFF_A1_LOW—0x96

Table 74: IIR_COEFF_A1_LOW—0x96

Bits	Name	Default	R/W	Description
7:0	A1[7:0]	0x00	R/W	IIR coefficient A1 lower byte.

IIR_COEFF_A1_HIGH—0x97**Table 75: IIR_COEFF_A1_HIGH—0x97**

Bits	Name	Default	R/W	Description
7:0	A1[15:8]	0x00	R/W	IIR coefficient A1 higher byte.

IIR_COEFF_A2_LOW—0x98**Table 76: IIR_COEFF_A2_LOW—0x98**

Bits	Name	Default	R/W	Description
7:0	A2[7:0]	0x00	R/W	IIR coefficient A2 lower byte.

IIR_COEFF_A2_HIGH—0x99**Table 77: IIR_COEFF_A2_HIGH—0x99**

Bits	Name	Default	R/W	Description
7:0	A2[15:8]	0x00	R/W	IIR coefficient A2 higher byte.

COEFF_IIR_G—0x9A**Table 78: COEFF_IIR_G—0x9A**

Bits	Name	Default	R/W	Description
7:6	Reserved	-	-	Reserved.
5:4	COEFF_IIR	0x0	R/W	The IIR in CX2081x is four-band. The Coeff_iir bit is used to set coefficients to a particular IIR: • Coeff_iir = 0 = Used to write coefficients to IIR0 • Coeff_iir = 1 = Used to write coefficients to IIR1
3	Reserved	-	-	Reserved.
2:0	G	0x0	R/W	IIR gain value register G.

IIR_EN—0x9B**Table 79: IIR_EN—0x9B**

Bits	Name	Default	R/W	Description
7:4	Reserved	0x00	-	Reserved.
3	ADC4_IIR_EN	0x0	R/W	adc4_iir enable: 0 = Disables the IIR 1 = Enables the IIR
2	ADC3_IIR_EN	0x0	R/W	adc3_iir enable: 0 = Disables the IIR 1 = Enables the IIR
1	ADC2_IIR_EN	0x0	R/W	adc2_iir enable: 0 = Disables the IIR 1 = Enables the IIR
0	ADC1_IIR_EN	0x0	R/W	adc1_iir enable: 0 = Disables the IIR 1 = Enables the IIR

Note:

- The B0, B1, B2, A1, A2, and G IIR coefficients are readable back only before they are modified. When they are written to memory and the coefficients are changed for another biquad, the coefficients that are written for the previous biquad are not readable.
- The IIR clock needs to be present for the IIR coefficients to be written into memory. Before starting to write the IIR coefficients, enable the IIR clock gating.

COEFF_LATCH_EN—0x9C**Table 80: COEFF_LATCH_EN—0x9C**

Bits	Name	Default	R/W	Description
7:4	Reserved	0x00	-	Reserved.
3	COEFF_LATCH_EN_ADC4	0x0	R/W	When set, the coefficient latch starts for the IIR set in Table 245 on page 254 . This register is cleared when read with the control interface and the memory store is done.
2	COEFF_LATCH_EN_ADC3	0x0	R/W	When set, the coefficient latch starts for the IIR set in Table 245 on page 254 . This register is cleared when read with the control interface and the memory store is done.
1	COEFF_LATCH_EN_ADC2	0x0	R/W	When set, the coefficient latch starts for the IIR set in Table 245 on page 254 . This register is cleared when read with the control interface and the memory store is done.
0	COEFF_LATCH_EN_ADC1	0x0	R/W	When set, the coefficient latch starts for the IIR set in Table 245 on page 254 . This register is cleared when read with the control interface and the memory store is done.

ATT_SEL—0x9D**Table 81: ATT_SEL—0x9D**

Bits	Name	Default	R/W	Description
7:6	ATT_SEL_ADC4	0x0	R/W	Programmable ATT SEL for ADC4: • 00 = 0dB attenuation • 01 = –6dB attenuation • 10 = –12dB attenuation • 11 = –18dB attenuation
5:4	ATT_SEL_ADC3	0x0	R/W	Programmable ATT SEL for ADC3: • 00 = 0dB attenuation • 01 = –6dB attenuation • 10 = –12dB attenuation • 11 = –18dB attenuation
3:2	ATT_SEL_ADC2	0x0	R/W	Programmable ATT SEL for ADC2: • 00 = 0dB attenuation • 01 = –6dB attenuation • 10 = –12dB attenuation • 11 = –18dB attenuation
1:0	ATT_SEL_ADC1	0x0	R/W	Programmable ATT SEL for ADC1: • 00 = 0dB attenuation • 01 = –6dB attenuation • 10 = –12dB attenuation • 11 = –18dB attenuation Note: This is actually not attenuation, but giving room for the gain to adjust. If the gain is not adjusted and programmed as above, the output is seen as attenuated.

I²C Control Interface

The devices feature an I²C control interface that allows access to the device registers, which are 8-bit addressed and have an 8-bit data width. Operation can be at either 100kHz (standard mode) or 400kHz (fast mode).

I²C Device Address Options

The device I²C address is 7 bits. The default I²C device address is 0x3B, but this can be changed to 0x35 using the I2C_DEV_ID0 device pin. An additional pair of I²C addresses are available for the CX20811 using the I2C_DEV_ID1 device pin.

Table 82: CX20810 I²C Device Address Options

I2C_DEV_ID0	I ² C Device Address
Low	0x3B
High	0x35

Table 83: CX20811 I²C Device Address Options

I2C_DEV_ID0	I2C_DEV_ID1	I ² C Device Address
Low	Low	0x3B
High	Low	0x35
Low	High	0x3C
High	High	0x36

Theory of Operation

Every byte put on the SDA line must be 8 bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the MSB first, as shown in the following figure.

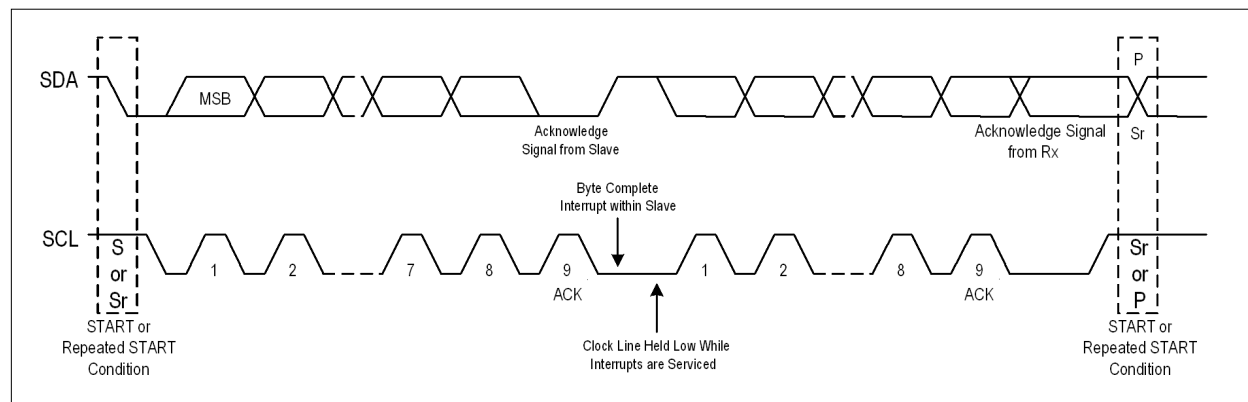


Figure 60: Transferring Data on I²C

A HIGH-to-LOW transition on the SDA line while the Serial Clock Line (SCL) is HIGH is a unique case. This situation indicates a START condition. A LOW-to-HIGH transition on the Serial Data (SDA) line while the SCL is HIGH defines a STOP condition. The START and STOP conditions are always generated by the master. The bus is considered to be busy after the START condition. The bus is considered to be free again a certain time after the STOP condition.

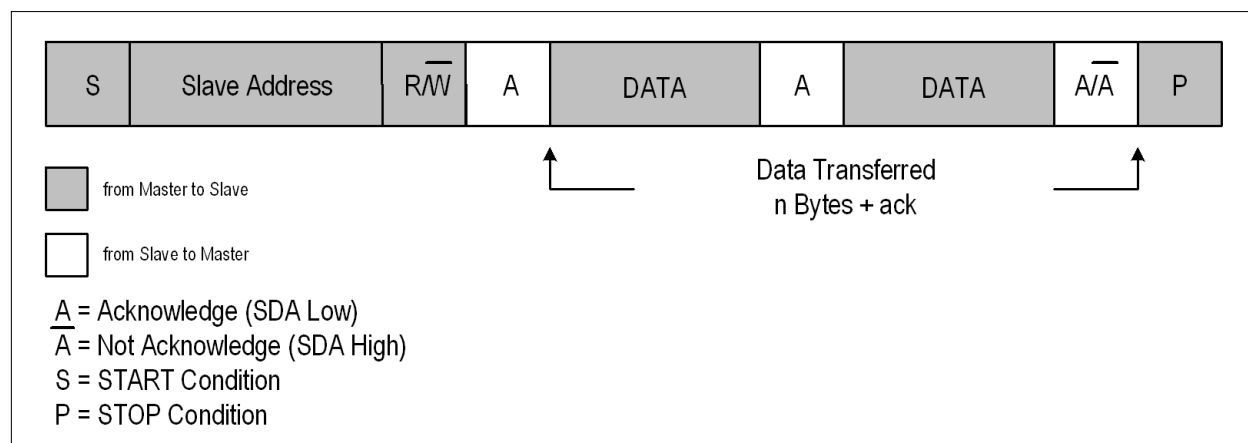


Figure 61: Data Transfer Format Example

Table 84: Slave Addressing Format for I²C

Slave Address	R/W Bit	Description
0000 000	0	General call address.
0000 000	1	Start byte.
0000 001	X	CBUS address.
0000 010	X	Reserved for a different bus format.
0000 011	X	Reserved.
0000 1XX	X	Hs mode master code.
1111 1XX	X	Reserved.
1111 0XX	X	10-bit slave addressing.

Clocking

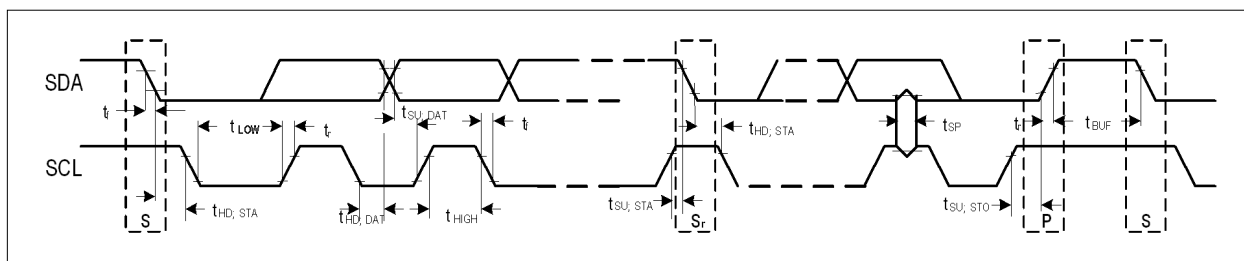


Figure 62: I²C Bus Timing

Table 85: I²C Timing Specifications

I²C (400kHz)	Symbol	Minimum	Maximum
Setup Time Start Condition	$t_{SU, STA}$	0.6 μ s	-
Hold Time Start Condition	$t_{HD, STA}$	0.6 μ s	-
SCL Clock LOW Period	t_{LOW}	1.3 μ s	-
SCL Clock HIGH Period	t_{HIGH}	0.6 μ s	-
Data Setup Time	$t_{SU, DAT}$	100ns	-
Data Hold Time	$t_{HD, DAT}$	0	0.9 μ s
Setup Time for STOP Condition	$t_{SU, STO}$	0.6 μ s	-

I²C Bus Operations

Write to the Slave Device

The following procedure describes how a host writes to the slave device.

1. Send a START sequence.
2. Send the I²C address of the slave with the R/W bit low.
3. Send the internal register address to be written to—send a high byte followed by a low byte.
4. Send the data byte.
5. Optional: Send any further data bytes using a burst operation.
6. Send the STOP sequence.

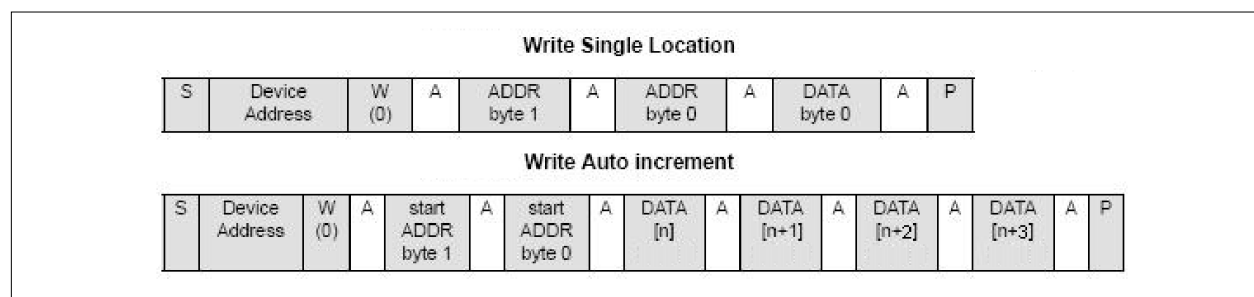


Figure 63: I²C Write Operations

Read from the Slave Device

The following procedure describes how a host reads from the slave device.

1. Send a START sequence.
2. Send the I²C address of the slave with the R/W bit low.
3. Send the internal register address to be written to—send a high byte followed by a low byte.
4. Send a START sequence again (repeated start).
5. Send the I²C address of the slave with the R/W bit high.
6. Read the data byte.
7. Optional: Send any further data bytes using a burst operation.
8. Send the STOP sequence.

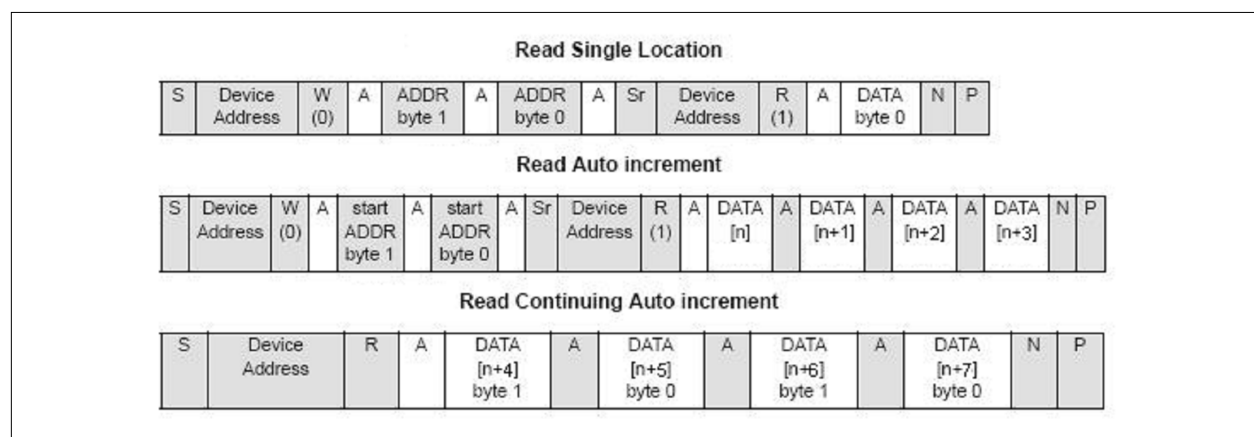


Figure 64: I²C Read Operations

PLL

General Description

All internal clocks are generated from a common internal source SYS_CLK. The SYS_CLK can be derived either directly from MCLK or from the internal PLLs.

Features

The CX20810/CX20811 supports being an:

- I²S master or slave when using a 900kHz to 50MHz input clock to the integrated PLL to derive SYS_CLK.
- I²S slave when not using the PLL, and the input clock must be 128*Fs, 256*Fs, or 512*Fs. Synaptics also supports the 24MHz special case.

Block Diagram

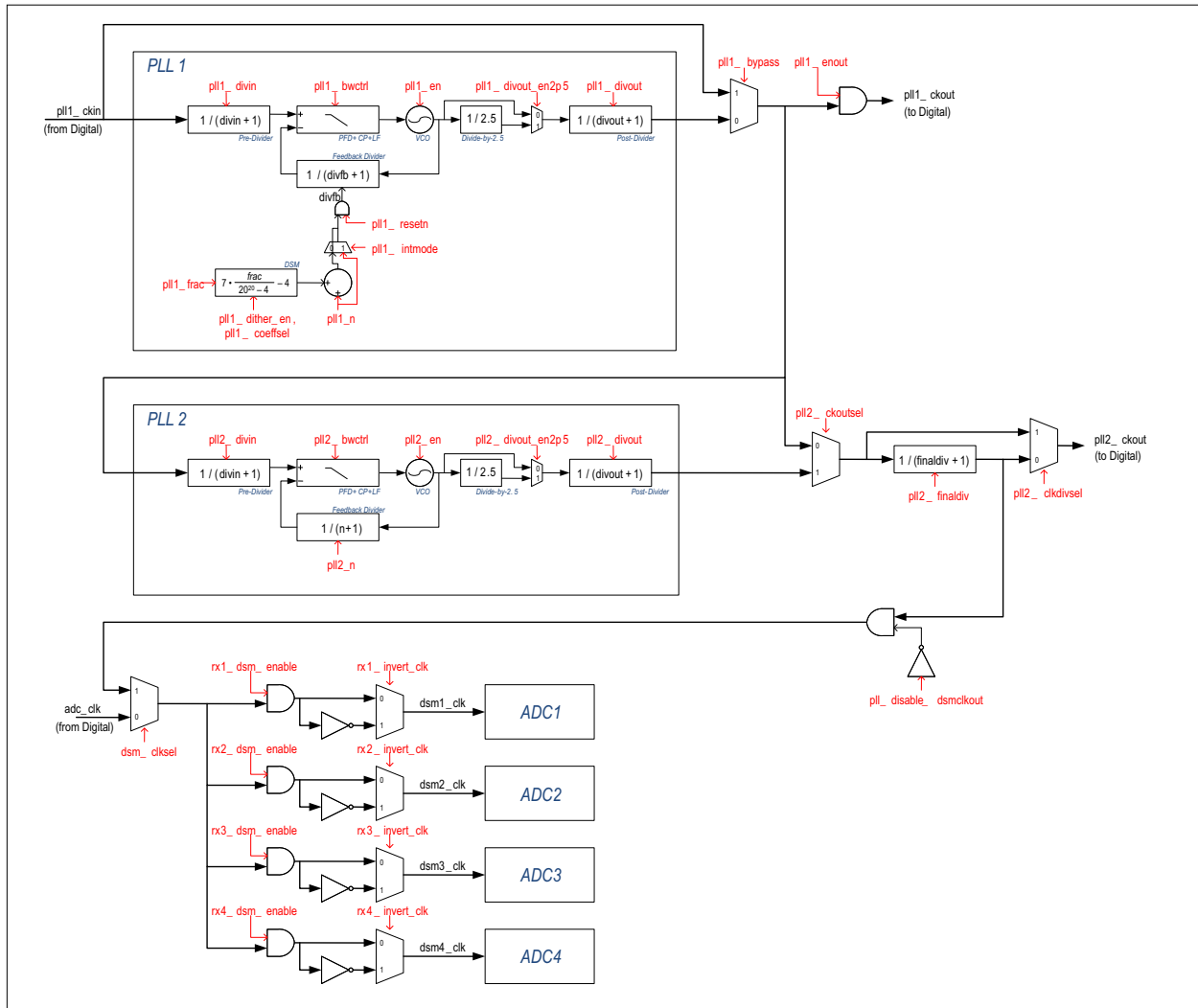


Figure 65: PLL Block Diagram

System Level Clocking Configurations

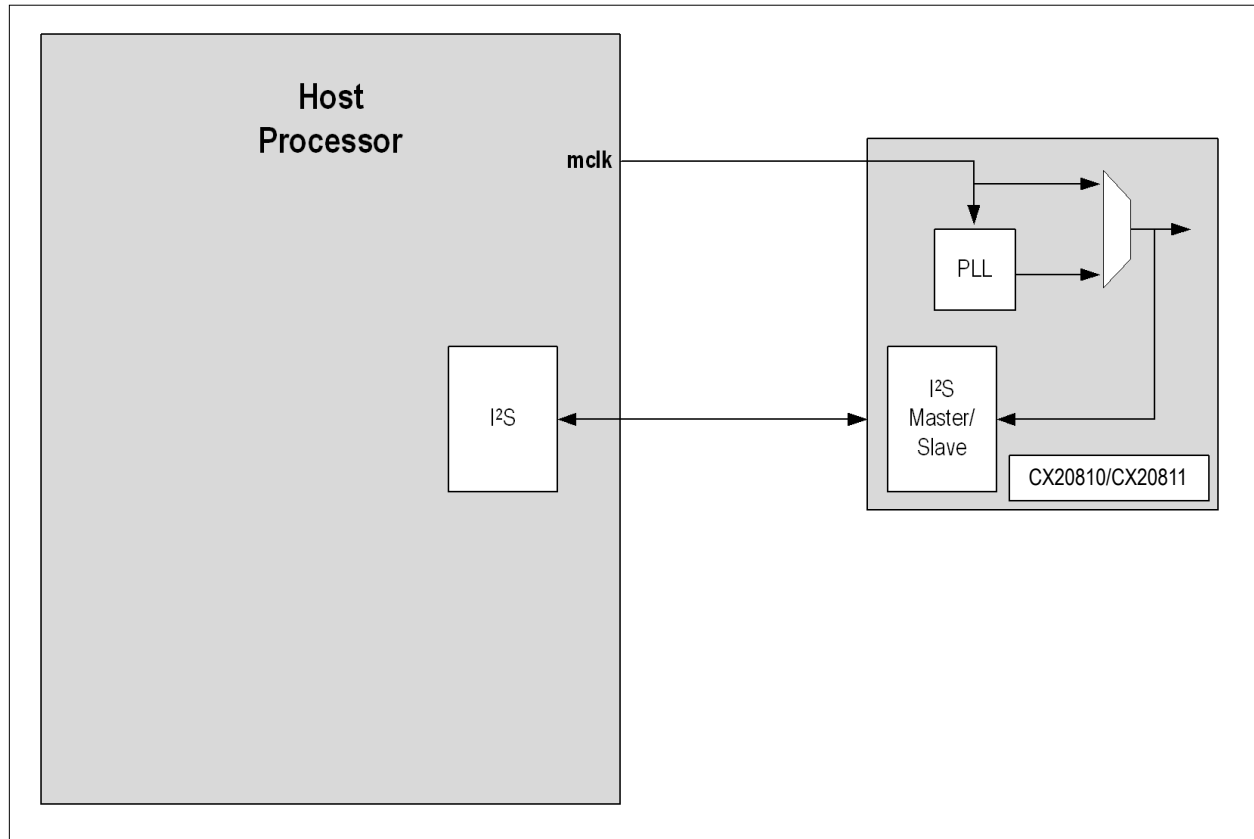


Figure 66: MCLK Input is Used for System Clocking

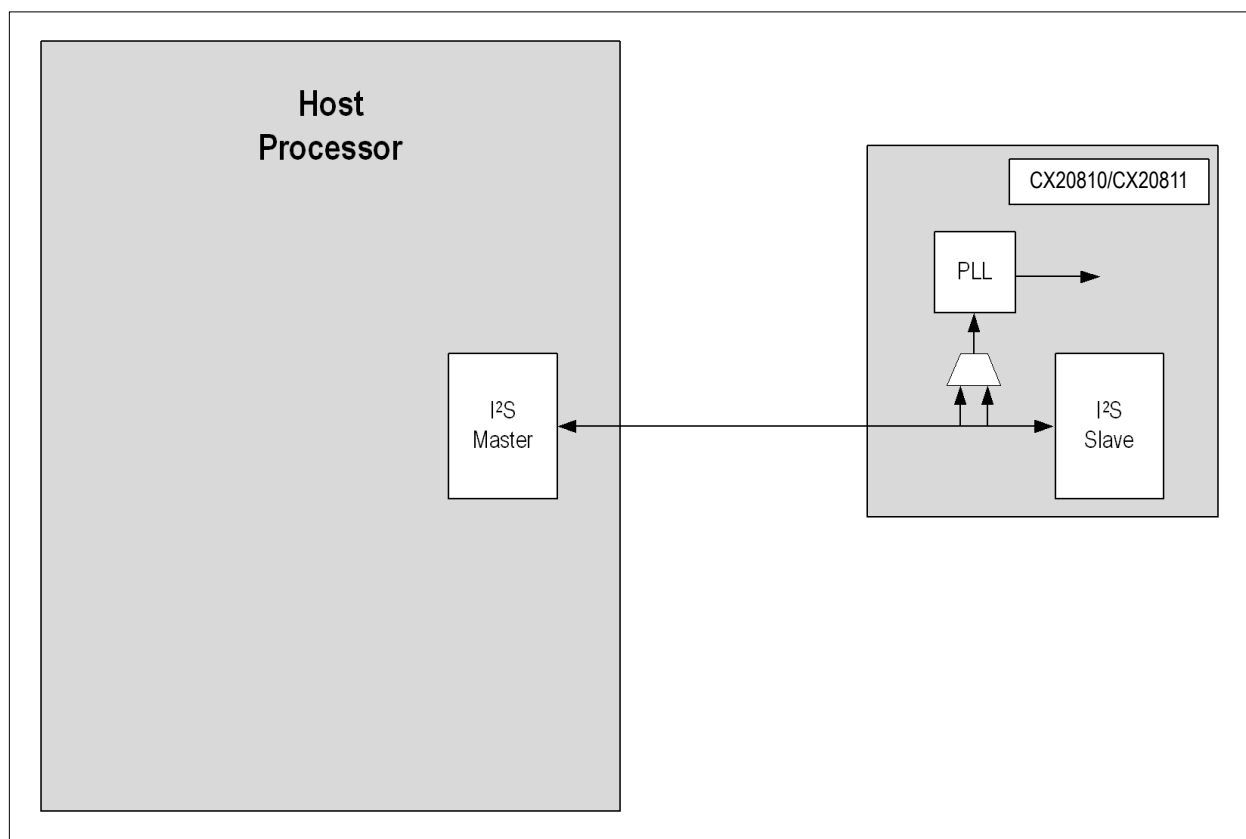


Figure 67: I²S Input is Used for System Clocking

PLL Scenarios

The following tables provide a few examples of what the PLL sources can be.

Table 86: PLL Scenarios

PLL Sources	Typical Clock Frequencies
MCLK	48MHz
	24MHz
	12MHz
	49.152MHz
	24.576MHz
	12.288MHz
	45.1584MHz
	22.5792MHz
	11.2986MHz
	19MHz
	27MHz
MCLK (Special Mode)	24MHz
I ² S Bit Clock	6.144MHz (Fs = 96kHz with 64-bits per frame)
	3.072MHz (Fs = 48kHz with 64-bits per frame)
	2.048MHz (Fs = 32kHz with 64-bits per frame)
	1.536MHz (Fs = 24kHz with 64-bits per frame)
	1.024MHz (Fs = 16kHz with 64-bits per frame)
	0.512MHz (Fs = 8kHz with 64 bits per frame)
	5.6448MHz (Fs = 88.2kHz with 64-bits per frame)
	2.8224MHz (Fs = 44.1kHz with 64-bits per frame)
	1.4112MHz (Fs = 22.05kHz with 64-bits per frame)
	3.072MHz (Fs = 96kHz with 32-bits per frame)
	1.536MHz (Fs = 48kHz with 32-bits per frame)
	1.024MHz (Fs = 32kHz with 32-bits per frame)
	0.768MHz (Fs = 24kHz with 32-bits per frame)
	0.512MHz (Fs = 8kHz with 32-bits per frame)
	0.256MHz (Fs = 16kHz with 32-bits per frame)
	2.8224MHz (Fs = 88.2kHz with 32-bits per frame)
	1.4112MHz (Fs = 44.1kHz with 32-bits per frame)
	0.705MHz (Fs = 22.05kHz with 32-bits per frame)

PLL Programming Specifications

Table 87: PLL Programming Specifications

Parameter	Minimum	Typical	Maximum	Units	Comments
Input Clock Frequency	Fckin	0.9	50	MHz	-
Pre-divider Ratio	-	1	256	Hz/Hz	Divider ratio equals the programming code in decimal +1.
Phase detector Frequency (Frequency at the Output of the Pre-divider)	Fcomp	0.9	8	MHz	-
Feedback Divider Ratio	-	1	512	Hz/Hz	In: - Integer mode = Divider ratio equals the programming code in decimal +1 for PLL2 and PLL1. - Fractional mode = Divider ratio is equal to integer part + fractional part + 1 for PLL1.
Integer Part of the Feedback Divider Ratio for the PLL1 in Fractional Mode	-	1	508	Hz/Hz	The pll1_n programs this parameter when in fractional mode. The divider ratio equals the programming code in decimal + 1.
Stable Range of the Fractional Part of the Feedback Divider Ratio for the PLL1 in Fractional Mode	-	-2.19	1.19	Hz/Hz	Decimal value of pll1_frac programs this according to the following equation: $7 \times \text{pll1_frac} / 2^{20} - 4, -4$
Stable Range of the Decimal Value of pll1_frac	-	271131	777441	-	-
Voltage-Controlled Oscillator (VCO) Frequency	Fvco	240	480	MHz	Equals the phase detector frequency multiplied by the feedback divider ratio when the PLL is locked.
Output Divider Ratio	-	1	8	Hz/Hz	Divider ratio equals the programming code in decimal +1.

PLL Programming Equations

- VCO frequency of PLL1 in integer mode:

$$\text{PLL1 Input Frequency} * ([\text{pll1_n} + 1] / [\text{pll1_divin} + 1])$$
- VCO frequency of PLL1 in fractional mode:

$$\text{PLL1 Input Frequency} * ([\text{pll1_n} + 7 * [\text{pll1_frac} / 2^{20-4}] - 3] / [\text{pll1_divin} + 1])$$
- PLL1 output frequency when pll1_divout_en2p5 is 0:

$$\text{PLL1 VCO Frequency} * (1 / [\text{pll1_divout} + 1])$$
- PLL1 output frequency when pll1_divout_en2p5 is 1:

$$\text{PLL1 VCO Frequency} * (1 / 2.5 * [\text{pll1_divout} + 1])$$
- VCO frequency of PLL2:

$$\text{PLL1 Output Frequency} * ([\text{pll2_n} + 1] / [\text{pll2_divin} + 1])$$
- PLL2 output frequency when pll2_divout_en2p5 is 0:

$$\text{PLL2 VCO Frequency} * (1 / [\text{pll2_divout} + 1])$$
- PLL2 output frequency when pll2_divout_en2p5 is 1:

$$\text{PLL2 VCO Frequency} * (1 / 2.5 * [\text{pll2_divout} + 1])$$

Loop Filter Tuning

For proper PLL operation, the phase detector frequency (i.e., the comparison frequency, which equals the clock frequency at the output of the pre-divider) should be at least five times higher than the loop BW. A ratio of 10 is preferred.

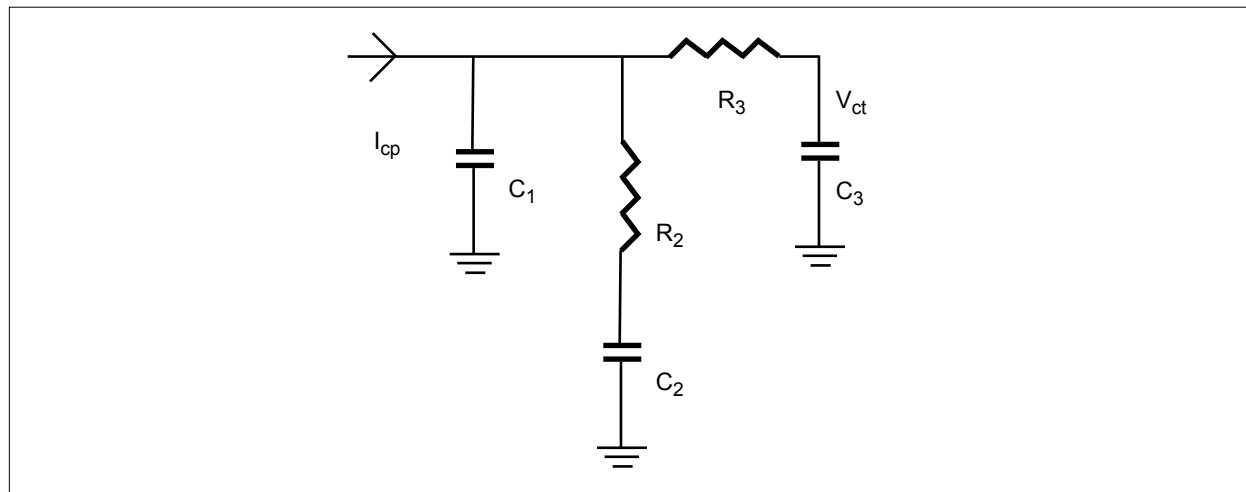


Figure 68: Loop Filter Tuning Phase Detector Frequency

Each PLL has a `bw_ctrl` register that adjusts the parameters in the loop filter—[Table 88](#) provides guidelines. The N value is the feedback divider ratio. A higher programming code mainly reduces the value of $R2$, which allows for smaller values of N while maintaining the phase margin. For a given value of N , a smaller programming code increases the loop BW at the expense of phase margin.

Table 88: Loop Filter Guidelines

Code	C1	C2	R2	R3	C3	BW	PM
00	0.5pF	34pF	100K	192kΩ	2 pF	130kHz @ N = 384	43
01	0.5pF	34pF	75K	64kΩ	1.5 pF	220kHz @ N = 180	56
10	0.5pF	34pF	50K	64kΩ	1.5 pF	410kHz @ N = 60	51
11	0.5pF	34pF	25K	64kΩ	1.5 pF	450kHz @ N = 30	45

Main Clocks

Table 89: Main Clocks

Clocks	Maximum Operating Frequency
MCLK	50MHz
AUDIO_PLL_O	49.152MHz
S_SCL	400kHz
RX_CLK	12.288MHz
TX_CLK	12.288MHz

Table 90: Derived Clocks

Clocks	Maximum Operating Frequency
SYS_CLK	12.288MHz
CLK_6P1	6.144MHz
I2S_TX_CLK	12.288MHz
I2S_RX_CLK	12.288MHz
OFFSET_CLK_SCAN	3.072MHz
OFFSET_CLK	1.536MHz

I²S Clocks

The following tables provide a few examples of the I²S clock in master mode for different sample rates. The source is PLL out or from the output of switch mux is shown in [Figure 65 on page 134](#).

Table 91: I²S Clock in Rx Master Mode

I ² S Rx Sample Rate	Rx Bit Clock (DAC)	PLL Clock
16kHz (BCLK/64)	1.024MHz (SYS_CLK/12)	12.288MHz
24kHz (BCLK/64)	1.536MHz (SYS_CLK/8)	12.288MHz
32kHz (BCLK/64)	2.048MHz (SYS_CLK/6)	12.288MHz
48kHz (BCLK/64)	3.072MHz (SYS_CLK/4)	12.288MHz
96kHz (BCLK/64)	6.144MHz (SYS_CLK/2)	12.288MHz
22.05kHz (BCLK/64)	1.44112MHz (SYS_CLK/8)	11.2896MHz
44.1kHz (BCLK/64)	2.8224MHz (SYS_CLK/8)	11.2896MHz
88.2kHz (BCLK/64)	5.6448MHz (SYS_CLK/4)	11.2896MHz

Table 92: I²S Clock in Tx Master Mode

I ² S Tx Sample Rate	Tx Bit Clock (ADC)	PLL Clock
16kHz (BCLK/64)	1.024MHz (SYS_CLK/12)	12.288MHz
24kHz (BCLK/64)	1.536MHz (SYS_CLK/8)	12.288MHz
32kHz (BCLK/64)	2.048MHz (SYS_CLK/6)	12.288MHz
48kHz (BCLK/64)	3.072MHz (SYS_CLK/4)	12.288MHz
22.05kHz (BCLK/64)	1.44112MHz (SYS_CLK/8)	11.2896MHz
44.1kHz (BCLK/64)	2.8224MHz (SYS_CLK/8)	11.2896MHz
88.2kHz (BCLK/64)	5.6448MHz (SYS_CLK/4)	11.2896MHz

PLL Programming Sequence

When programming the PLL, there is a generalized sequence that should be followed when writing the registers. Enabling of the PLLs, digital input clock divider, and clock gate should all be performed after other PLL settings have been programmed. The following procedure describes the generalized sequence.

1. Program the PLL1/PLL2 values using the 0x60 through 0x69 registers, excepting bits that are set below.
2. Enable the individual PLLs as needed.
 - a. Enable PLL1 using the 0x60 [1:0] register (set a value of **11b** to enable PLL1).
 - b. Enable PLL2 using the 0x67 [0] register (set a value of **1b** to enable PLL2).
3. Set the digital divider using the 0x0D [2:0] register as needed.
 - a. Set 0x0D [2] = 0 and 0x0D [1:0] to the desired divide values.
 - b. Set 0x0D [2] = 1 to latch the divide ratio into the devices.
4. Enable the clock gating to the PLLs using the 0x0D [3] register (set a value of **1b** to enable the clocks).

Register Set

Table 93: Register Set

Register Name	Register Address (Hex)	Default (Hex)
MCLK_CTRL	0x08	0x00
PLL_CLK_CTRL	0x09	0x00
I2S_TX_CLK_CTRL	0x0A	0x0B
I2S_RX_CLK_CTRL	0x0B	0x03
I2S_CLK_CTRL	0x0C	0x08
PLL_DIV_CTRL	0x0D	0x03
PWM_CLK_CTRL	0x0E	0x00
SOFT_RST_CTRL	0x0F	0x00
PLL_CTRL_1	0x60	0x00
PLL_CTRL_2	0x61	0x00
PLL_CTRL_3	0x62	0x00
PLL_CTRL_4	0x63	0x00
PLL_CTRL_5	0x64	0x00
PLL_CTRL_6	0x65	0x00
PLL_CTRL_7	0x66	0x00
PLL_CTRL_8	0x67	0x00
PLL_CTRL_9	0x68	0x00
PLL_CTRL_10	0x69	0x00

MCLK_CTRL—0x08**Table 94: MCLK_CTRL—0x08**

Bits	Name	Default	R/W	Description
7	Reserved	0	-	Reserved.
6	MCLK_CTRL [6]	0	R/W	Clock to the register block to latch the status of the GPIO and so forth: 0 = CODEC_clk_d2d 1 = Reserved
5	MCLK_CTRL [5]	0	R/W	MCLK gate enable to the entire chip: 0 = Gates the clock 1 = Enables the clock
4	MCLK_CTRL [4]	0	R/W	0 = MCLK from the pin feeds the PLL 1 = MCLK from the programmable divider feeds the PLL
3	MCLK_CTRL [3]	0	R/W	Enable for the MCLK divisor change. The programmable divider change is done through steps. Change the divisor value in MCLK_CTRL [2:0] and then set this bit = 0 → 1 to enable the divisor change.
2:0	MCLK_CTRL [2:0]	0	R/W	Divided version of MCLK (MCLK_CTRL [2:0] + 1). The source clock is MCLK. Values are from 2–8. If programmed for value of 0 or 1, the divider output is MCLK/2.

PLL_CLK_CTRL—0x09**Table 95: PLL_CLK_CTRL—0x09**

Bits	Name	Default	R/W	Description
7:6	PLL_CLK_CTRL [7:6]	0	R/W	Selects MCLK or the bit clock to feed the PLL: 00 = MCLK or divided version of MCLK 01 = I2S Tx bit clock 10 = I2S Rx bit clock 11 = GPIO3 (test mode using dtest4[3])
5:3	Reserved	0	-	Reserved.
2:1	PLL_CLK_CTRL [2:1]	0	R/W	Main clock for digital blocks: 00 = PLL 01 = MCLK or divided version of MCLK 10 = Reserved 11 = PLL divided version
0	PLL_CLK_CTRL [0]	0	R/W	Used to gate the main clock for the DSP. The clock selected by the mux select of PLL_CLK_CTRL [2:1] is gated: 0 = Gate for the DSP clocks and audio data interface clocks 1 = Clock enable for DSP clocks and audio data interface clocks

I2S_TX_CLK_CTRL—0x0A**Table 96: I2S_TX_CLK_CTRL—0x0A**

Bits	Name	Default	R/W	Description
7	I2S_TX_CLK_CTRL [7]	0	R/W	Enable for the divisor change of the I ² S/DSP Tx in master mode. First set the divisor value in I2S_TX_CLK_CTRL [6:0], and then set this bit = 0-to-1 to enable the divisor change.
6:0	I2S_TX_CLK_CTRL [6:0]	0x0B	R/W	I ² S/DSP Tx clock divide control source clk/ (I2S_TX_CLK_CTRL [6:0] + 1). The source clock can be either PLL or MCLK, based on the PLL_CLK_CTRL [2:1] register.

I2S_RX_CLK_CTRL—0x0B**Table 97: I2S_RX_CLK_CTRL—0x0B**

Bits	Name	Default	R/W	Description
7	I2S_RX_CLK_CTRL [7]	0	R/W	Enable for the divisor change of the I ² S/DSP Rx in master mode. First set the divisor value in I2S_RX_CLK_CTRL [6:0], and then set this bit = 0-to-1 to enable the divisor change.
6:0	I2S_RX_CLK_CTRL [6:0]	0x03	R/W	I ² S/DSP Rx clock divide control source CLK/ (I2S_RX_CLK_CTRL [6:0] + 1). The source clock can be either PLL or MCLK, based on the PLL_CLK_CTRL [2:1] register.

I2S_CLK_CTRL—0x0C**Table 98: I2S_CLK_CTRL—0x0C**

Bits	Name	Default	R/W	Description
7	Reserved	0	-	Reserved.
6	I2S_CLK_CTRL [6]	0	R/W	Polarity of the I ² S/DSP Rx clock can be inverted: 0 = Default value 1 = Inverts the polarity Note: The Rx clock should be inverted in the DSP Rx mode.
5	I2S_CLK_CTRL [5]	0	R/W	I ² S/DSP Rx clock gate enable: 0 = Gates the clock 1 = Enables the clock
4	I2S_CLK_CTRL [4]	0	R/W	Selects I ² S/DSP Rx in master/slave mode: 0 = Slave mode 1 = Master mode
3	I2S_CLK_CTRL [3]	1	R/W	Clock gating for ADC3 and ADC4 First In, First Out (FIFO) items in the I ² S/DSP module: 0 = Gate the clock to the ADC3/4 FIFOs 1 = Clock enable to the ADC3/4 FIFOs
2	I2S_CLK_CTRL [2]	0	R/W	Controls polarity of the internal clock applied to the interface engine (relative to BCLK) 0 = Internal clock is inverted version of BCLK 1 = Internal clock is non-inverted version of BCLK Note: In slave mode, LRCK is sampled on the clock edge that is opposite to the clock edge that launches DATA. Bit setting 0 is used when LRCK should be sampled on the rising edge of BCLK. Bit setting 1 is used when LRCK needs to be sampled on the falling edge of BCLK. See "I2S/TDM Slave Mode" on page 163 for more information.
1	I2S_CLK_CTRL [1]	0	R/W	I ² S/DSP Tx clock gate enable: 0 = Gates the clock 1 = Enables the clock
0	I2S_CLK_CTRL [0]	0	R/W	Selects the I ² S/DSP Tx in master/slave mode: 0 = Slave mode 1 = Master mode

PLL_DIV_CTRL—0x0D**Table 99: PLL_DIV_CTRL—0x0D**

Bits	Name	Default	R/W	Description
7:4	Reserved	0	-	Reserved.
3	PLL_DIV_CTRL [3]	0	R/W	PLL divider output gate enable to the entire chip: 0 = Gates the clock 1 = Enables the clock
2	PLL_DIV_CTRL [2]	0	R/W	Enable for the PLL divisor change. The programmable divider change is done through steps. Change the divisor value in PLL_DIV_CTRL [1:0], and then set this bit = 0 → 1 to enable the divisor change.
1:0	PLL_DIV_CTRL [1:0]	3	R/W	Divided version of the audio PLL (PLL_DIV_CTRL [1:0] +1). The source clock is the audio PLL. Divide values of 2, 3, or 4 are available: 00b = pll_clk/2 (/1 is not available) 01b = pll_clk/2 10b = pll_clk/3 11b = pll_clk/4 See Table 140 on page 194 to bypass this divider if desired.

PWM_CLK_CTRL—0x0E**Table 100: PWM_CLK_CTRL—0x0E**

Bits	Name	Default	R/W	Description
7:4	Reserved	-	-	Reserved.
3	PWM_CLK_CTRL[3]	0	R/W	Clock gate for DC detection counter: 0 = Gated 1 = Enables the clock for the DC detection counter
2	PWM_CLK_CTRL[2]	0	R/W	Clock gating for the DC detection filter: 0 = Gated 1 = Enables the clock
1	PWM_CLK_CTRL[1]	0	R/W	Clock gating for the PWM clock out to the analog PWM driver: 0 = Gated 1 = Enables the clock
0	PWM_CLK_CTRL[0]	0	R/W	Clock gating for the DAC/PWM digital engine: 0 = Gated 1 = Enables the clock

Note: For DC detection both [3:2] need to be enabled

SOFT_RST_CTRL—0x0F**Table 101: SOFT_RST_CTRL—0x0F**

Bits	Name	Default	R/W	Description
7:2	Reserved	-	-	Reserved.
1	SOFT_RST_CTRL[1]	0	R/W	When set to 1, sets all the values in the registers to their default values.
0	SOFT_RST_CTRL[0]	0	R/W	When set to 1, clears all the DSP and audio data interface values.

PLL_CTRL_1—0x60**Table 102: PLL_CTRL_1—0x60**

Bits	Name	Default	R/W	Description
7	PLL1_DIVOUT_EN2P5	0	R/W	Enables an additional divide-by-2.5 on the PLL1 output.
6:4	PLL1_DIVOUT	0	R/W	Output divider selection for PLL1—divide ratio = pll1_divout+1.
3	PLL1_N[8]	0	R/W	MSB of the 9-bit integer part of the PLL1 feedback divider.
2	PLL1_BYPASS	0	R/W	Bypasses PLL1: 0 = Clock output is from the PLL1 output 1 = Clock output is from the CODEC digital
1	PLL1_RESETN	0	R/W	Active-low reset for PLL1 (1 = enable).
0	PLL1_EN	0	R/W	Enables PLL1 (1 = enable).

PLL_CTRL_2—0x61**Table 103: PLL_CTRL_2—0x61**

Bits	Name	Default	R/W	Description
7:0	PLL1_N[7:0]	0	R/W	Eight LSBs of the 9-bit integer part of the PLL1 feedback divider—divide ratio = pll1_n + 1.

PLL_CTRL_3—0x62**Table 104: PLL_CTRL_3—0x62**

Bits	Name	Default	R/W	Description
7:6	PLL1_BWCTRL	0	R/W	Loop filter tuning.
5:0	PLL1_DIVIN	0	R/W	Input divider selection for the PLL1 divide ratio = pll1_divin + 1.

PLL_CTRL_4—0x63*Table 105: PLL_CTRL_4—0x63*

Bits	Name	Default	R/W	Description
7:2	PLL1_COEFFSEL	0	R/W	Tune feedback coefficients in the PLL1 fractional modulator.
1	PLL1_DITHER_EN	0	R/W	Enables the dither for PLL1 (1 = enable).
0	PLL1_INTMODE	0	R/W	Enables the integer-only mode for PLL1 (1 = disable fractional modulator).

PLL_CTRL_5—0x64*Table 106: PLL_CTRL_5—0x64*

Bits	Name	Default	R/W	Description
7:0	PLL1_Frac[7:0]	0	R/W	Eight LSBs of the fractional part of the PLL1 feedback divider.

PLL_CTRL_6—0x65*Table 107: PLL_CTRL_6—0x65*

Bits	Name	Default	R/W	Description
7:0	PLL1_Frac[15:8]	0	R/W	Bits 15 to 8 of the fractional part of the PLL1 feedback divider.

PLL_CTRL_7—0x66*Table 108: PLL_CTRL_7—0x66*

Bits	Name	Default	R/W	Description
7	PLL2_CKDIVSEL	0	R/W	Bypasses the final output divider for pll2_ckout: 0 = pll2_ckout is the output of the final output divider 1 = pll2_ckout is the input of the final output divider
6:4	PLL2_FINALDIV	0	R/W	The pll2_ckout final output divider control divide ratio = pll2_finaldiv+1.
3:0	PLL1_FRAC[19:16]	0	R/W	Four MSBs of the fractional part of the PLL1 feedback divider.

PLL_CTRL_8—0x67*Table 109: PLL_CTRL_8—0x67*

Bits	Name	Default	R/W	Description
7	PLL2_DIVOUT_EN2P5	0	R/W	Enables the additional divide-by-2.5 on the PLL2 output.
6:4	PLL2_DIVOUT	0	R/W	Output divider selection for the PLL2 divide ratio = pll2_divout+1.
3	PLL2_N[8]	0	R/W	MSB of the 9-bit integer part of the PLL2 feedback divider.
2	PLL2_CKOUTSEL	0	R/W	Selects the pll2_ckout clock source: 0 = pll2_ckout is the output of PLL1 1 = pll2_ckout is the output of PLL2
1	PLL1_ENOUT	0	R/W	Enables the pll1_ckout output to the CODEC digital.
0	PLL2_EN	0	R/W	Enables PLL2 (1 = enable).

PLL_CTRL_9—0x68*Table 110: PLL_CTRL_9—0x68*

Bits	Name	Default	R/W	Description
7:0	PLL2_N[7:0]	0	R/W	Eight LSBs of the 9-bit integer part of the PLL2 feedback divider—divide ratio = pll2_n + 1.

PLL_CTRL_10—0x69*Table 111: PLL_CTRL_10—0x69*

Bits	Name	Default	R/W	Description
7:6	PLL2_BWCTRL	0	R/W	Loop filter tuning.
5:0	PLL2_DIVIN	0	R/W	Input divider selection for the PLL2—divide ratio = pll2_divin + 1.

Digital Audio Data Interface

The CX20810/CX20811 features a highly-configurable digital audio data interface. Synaptics supports the following four interface formats:

- I²S
- Left-justified
- Right-justified
- DSP/PCM

The CX20810/CX20811 supports either a seven-wire or five-wire mode for each of the four interface formats. The PCM operation is supported using the DSP mode.

Time-Division Multiplexing (TDM) is available in all four data format modes. The TDM allows multiple devices to transfer data simultaneously on the same bus. The CX20810/CX20811 ADCs and DAC (CX20811 only) support TDM in master and slave modes for all data formats and word lengths. The TDM mode is enabled by using the I2S_DSP_SEL register bit (see the registers in "I2S Clocking" on page 175).

The digital audio data interface supports the following sample rates:

- 8kHz
- 16kHz
- 24kHz
- 32kHz
- 44.1kHz
- 48kHz
- 96kHz

The supported sample widths are 8-bit, 16-bit, and 24-bit.

In seven-wire mode, the Tx clocks are independent from the Rx clocks. The Tx and Rx can each independently be either master or slave. The seven-wire mode I²S interface signals consist of:

- TX_DATA_1
- TX_DATA_2
- TX_BCLK
- TX_WS
- RX_DATA
- RX_BCLK
- RX_WS

In five-wire mode, the clocks are shared by both the Tx and Rx. The Tx and Rx must both be master or slave. The five-wire mode I²S interface signals consist of:

- TX_DATA_1
- TX_DATA_2
- BCLK
- WS
- RX_DATA

Note: Because the CX20810/CX20811 devices are 24 bits, the eight LSBs are ignored if operated in 32-bit mode on the Rx side and are not driven on the Tx side. In this case, Synaptics recommends to add a pull-down resistor, if necessary, to the TX_DATA_1 line and the RX_DATA line in TDM mode.

Block Diagram

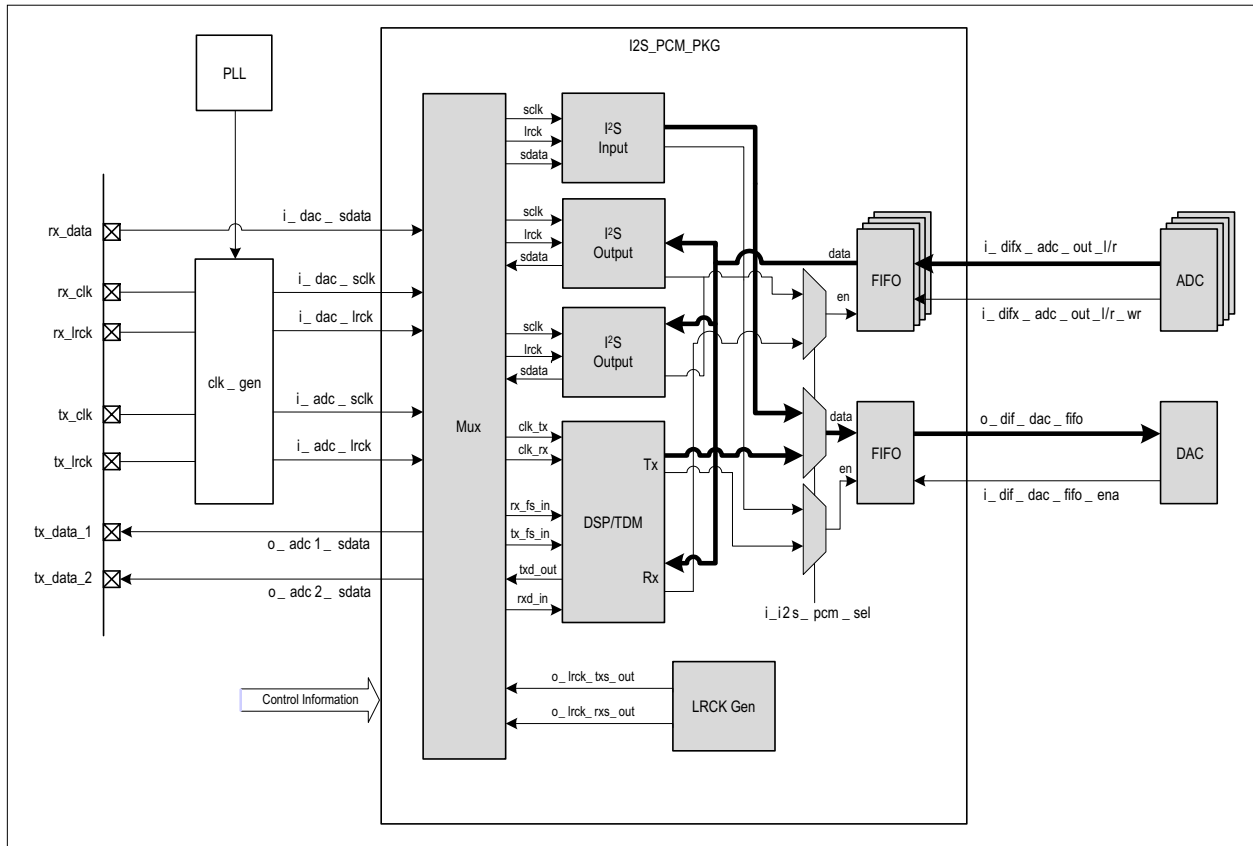


Figure 69: Digital Audio Interface Block Diagram

Theory of Operation

This section provides the definitions of different modes and register settings required to configure a specific mode.

Note: Each mode can be operated in normal mode or TDM mode. When no specific mode is mentioned, the normal mode takes priority.

I²S

The I²S bus has three types of wires:

- Serial Bit Clock (BCLK)
- Left/Right Clock (LRCK)/Word Strobe (WS) for data alignment
- Serial data

The serial data and WS wires are always driven on the negative edge of the BCLK. The MSB of data is transmitted first.

The CX20810/CX20811 supports four ADC channels and one DAC (CX20811 only) channel. Accordingly there are two I²S ADC serial output data lines and one I²S DAC serial input data line. One serial data line supports two channels. The audio interface can operate in normal and TDM modes.

In TDM mode, all four ADC channels of data transmit on TX_DATA_1. The default I²S operational mode uses seven wires. The I²S can be configured to work in five-wire mode by multiplexing the BCLK and LRCK signals if the ADCs and DAC are all running at the same clock rate and sample rates. Either ADC BCLK/LRCK or DAC BCLK/LRCK can be chosen during the five-wire mode.

In normal mode, ADC1 and ADC2 data is sent on TX_DATA_1. The ADC3 and ADC4 data is sent on the TX_DATA_2 line. The I²S TX_DATA_1 and TX_DATA_2 path lines can be individually enabled or disabled. In case of an application that only uses ADC1 and ADC2, clocks to the ADC3 and ADC4 FIFOs can be gated by disabling the I2S_CLK_CTRL[3] register bit along with disabling I2S2_TX_EN.

Table 112: I²S Modes and Register Settings

I ² S Signal	Seven-Wire Mode	Five-Wire Mode (DAC)	Five-Wire Mode (ADC)	Top Level Wire
DAC Serial Clock	Available	Available	Same as ADC Serial Clock	RX_CLK
DAC LRCK	Available	Available	Same as ADC LRCK	RX_LRCK
DAC Serial Data	Available	Available	Available	RX_DATA
ADC Serial Clock	Available	Same as DAC Serial Clock	Available	TX_CLK
ADC LRCK	Available	Same as DAC LRCK	Available	TX_LRCK
ADC Serial DATA1	Available	Available	Available	TX_DATA_1
ADC Serial DATA2	Available	Available	Available	TX_DATA_2

The I²S protocol uses the LRCK to define whether the data is being transmitted for the left or right channel. The LRCK is low for the left channel and high for the right channel. The LRCK does not need to be symmetrical. There is a delay of one clock bit from the time the LRCK signal changes state to the first data bit (MSB) on the data line. The data is written MSB first and is valid on the rising edge of the bit clock. When the programmed sample width is taken, any remaining bits are ignored.

I²S Normal Mode

To configure the audio interface to I²S normal mode, select I2S_DSP_SEL bit LOW. The I2S_TX_CTRL_1 through I2S_RX_CTRL_2 registers are used to configure specific usage scenarios.

- I2S_TX_MODE_SEL and I2S_RX_MODE_SEL are set to 0x00
- TX_WS_WID, RX_WS_WID, TX_FRM_LEN, and RX_FRM_LEN are used to describe the LRCK and frame length relation

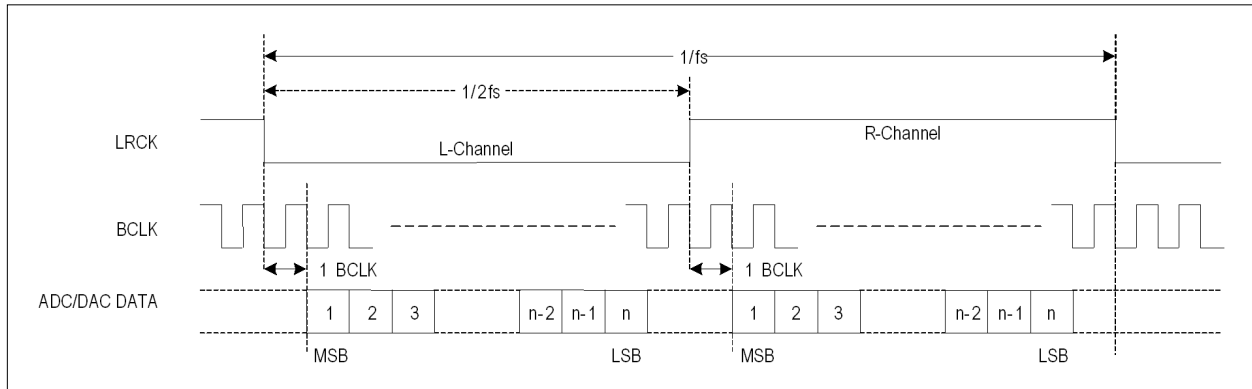


Figure 70: I²S Justified Audio Interface (Assuming n-Bit Word Length)

I²S Time-Division Multiplexing (TDM) Mode

To configure the audio interface to I²S TDM mode, select I2S_DSP_SEL bit HIGH.

- Set the DSP_TX_WSPOL and DSP_RX_WSPOL bits to HIGH
- Set the DSP_DSTART_DLY, DSP_TX_OUT_LINE_SEL, and DSP_TX_TRI_N bits to HIGH

The DSP_CTRL through DSP_RX_CTRL_1 registers are used to configure specific usage scenarios. The TX_WS_WID, RX_WS_WID, TX_FRM_LEN, and RX_FRM_LEN bits are used to describe the LRCK and frame length relation.

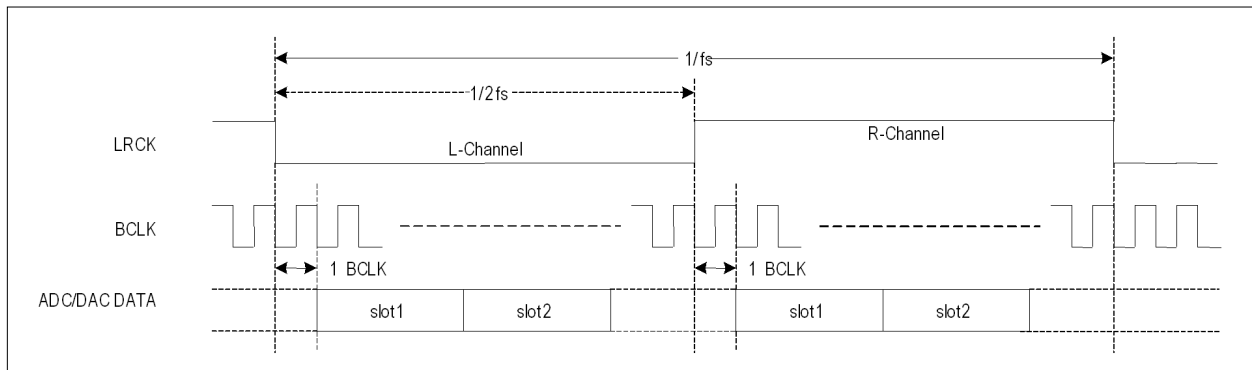


Figure 71: I²S Justified Audio Interface in TDM Mode

Left-Justified

Left-Justified—I²S Mode

Left-justified mode is a special case of the I²S mode. The LRCK is high for the left channel and low for the right channel. The MSB appears on the data line following the LRCK transition on the same BCLK. The data is written MSB first and is valid on the rising edge of bit clock. When the programmed sample width is taken, any remaining bits are ignored. If the LRCK toggles before the full word length is read, the remaining bits are zeroed.

To program the audio interface to left-justified normal mode, select I2S_DSP_SEL bit LOW. The I2S_TX_CTRL_1 through I2S_RX_CTRL_2 registers are used to configure specific usage scenarios.

- I2S_TX_MODE_SEL and I2S_RX_MODE_SEL are set to 0x01
- TX_WS_WID, RX_WS_WID, TX_FRM_LEN, and RX_FRM_LEN are used to describe the LRCK and frame length relation

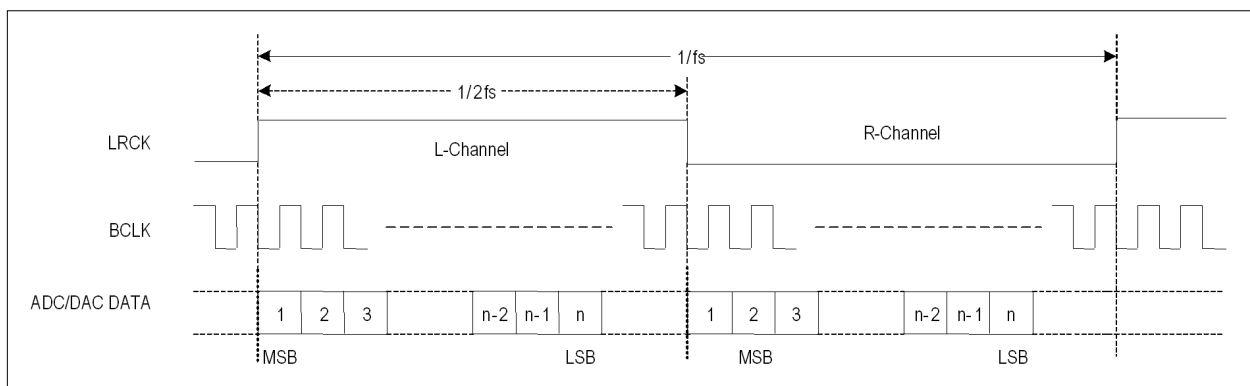


Figure 72: Left-Justified Audio Interface (Assuming n-Bit Word Length)

Left-Justified—TDM Mode

To program the audio interface to left-justified TDM mode:

- Select I2S_DSP_SEL bit HIGH
- Set the DSP_TX_WSPOL and DSP_RX_WSPOL bits to LOW
- Set DSP_DSTART_DLY to LOW
- Set the DSP_TX_OUT_LINE_SEL and DSP_TX_TRI_N bits to HIGH

The DSP_CTRL through DSP_RX_CTRL_1 registers are used to configure specific usage scenarios.

The TX_WS_WID, RX_WS_WID, TX_FRM_LEN, and RX_FRM_LEN are used to describe the LRCK and frame length relation.

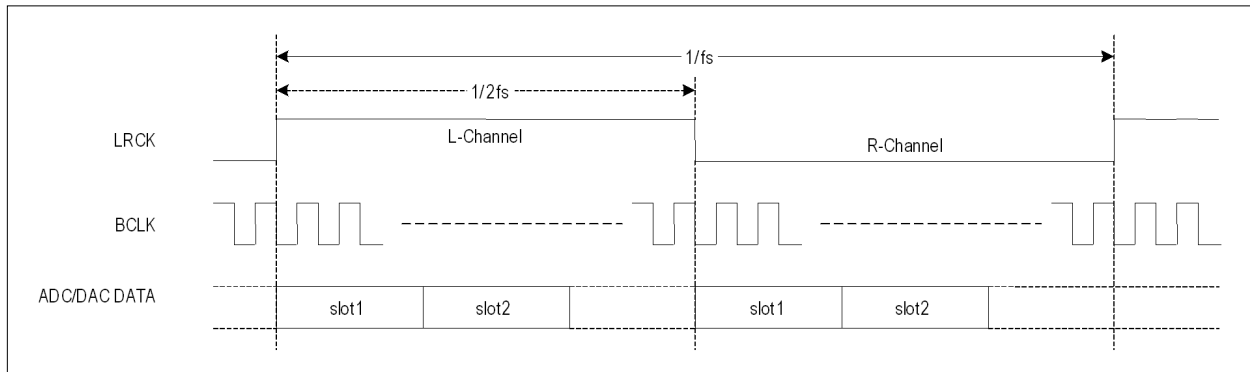


Figure 73: Left-Justified Audio Interface in TDM Mode

Right-Justified

Right-Justified—I²S Mode

Right-justified mode is a special case of the I²S mode. Similar to left-justified mode, LRCK is high for the left channel and low for the right channel.

In right-justified mode, the LSB of data is always clocked by the last bit clock before the LRCK transitions. Data is captured in a 24-bit shift register until LRCK toggles, and then the last 24, 16, or 8 bits are transferred to the channel indicated by the previous state of LRCK. The data is written MSB first, and is valid on the rising edge of bit clock. All leading bits are ignored. The number of bit clock delays for the first valid data bit from the toggle of LRCK is programmable through the I2S_TX/RX_BCNT_DLY field. Although the bit count delay field is programmable, the right-justified mode data is optimum when the valid data bits are shifted to an extent where the LSB of data is clocked by the last bit clock before LRCK toggles.

To program the audio interface to right-justified normal mode, select I2S_DSP_SEL bit LOW. The I2S_TX_CTRL_1 through I2S_RX_CTRL_2 registers are used to configure specific usage scenarios.

- I2S_TX_MODE_SEL and I2S_RX_MODE_SEL are set to 0x02
- TX_WS_WID, RX_WS_WID, TX_FRM_LEN, and RX_FRM_LEN are used to describe the LRCK and frame length relation

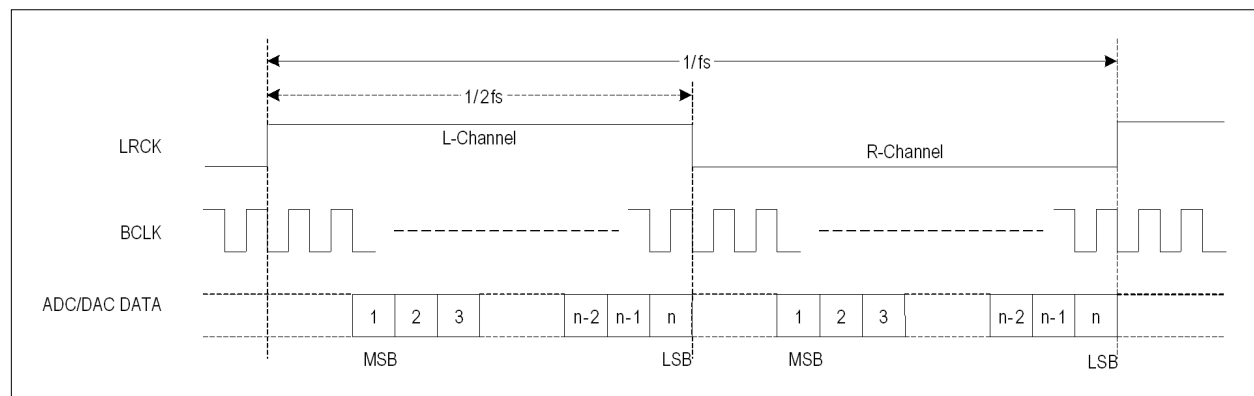


Figure 74: Right-Justified Audio Interface (Assuming n-Bit Word Length)

Right-Justified—TDM Mode

To program the audio interface to right-justified TDM mode:

- Select the I2S_DSP_SEL bit to HIGH
- Set the DSP_TX_WSPOL and DSP_RX_WSPOL bits to LOW
- Set the DSP_DSTART_DLY bit to LOW
- Set the DSP_TX_OUT_LINE_SEL and DSP_TX_TRI_N bits to HIGH

The DSP_CTRL through DSP_RX_CTRL_1 registers are used to configure specific usage scenarios. The TX_WS_WID, RX_WS_WID, TX_FRM_LEN, and RX_FRM_LEN bits are used to describe the LRCK and frame length relation.

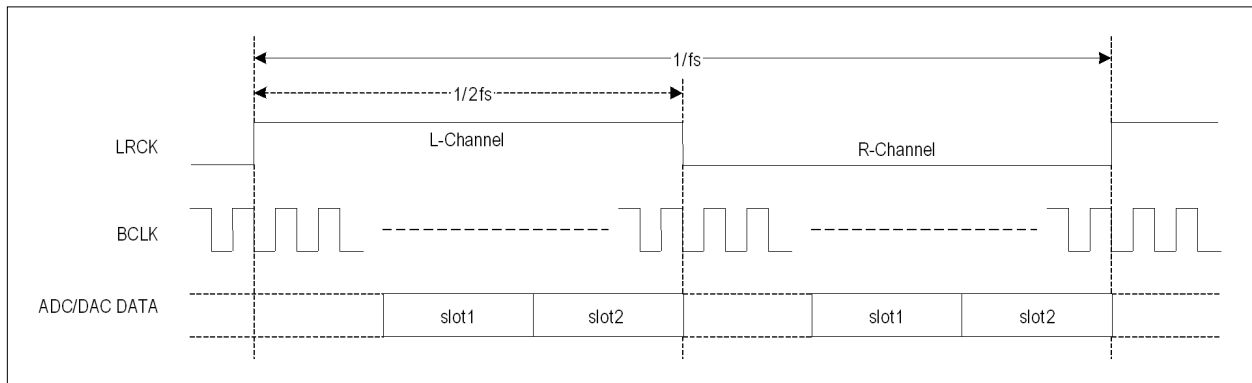


Figure 75: Right-Justified Audio Interface in TDM Mode

Digital Signal Processor (DSP) Mode

The DSP mode has three signals:

- Serial clock
- Frame sync pulse (or LRCK)
- Serial data line

The serial data and frame sync pulse are driven on the positive edge of the serial clock. On the DAC path, the CX20811 DSP has the following set of signals:

- Bclock
- Frame sync pulse
- Serial data-in

On the ADC path, the CX20810/CX20811 DSP has the following set of signals:

- Bclock
- Frame sync pulse
- Serial data-out1
- Serial data-out2

Data is sent/received as slots on the serial data. Each slot is 8 bits wide. Depending on the sample width, each channel can occupy one or more slots.

Example: A 24-bit channel occupies three slots.

To accommodate the four ADC channels and 1 DAC channel, the CX20810/CX20811 supports one, four-channel half-duplex DSP. The DAC data is received on DSP serial data-in. The ADC data is sent on both DSP serial data-outs. Data from ADC1/2 is sent on DSP serial data-out1, and data from ADC3/4 is sent on DSP serial data-out2. The DSP can also be configured to send all the ADC channel data on DSP serial data-out1 (through DSP_TX_OUT_LINE_SEL field).

In default DSP operational mode, there are seven wires. The DSP can be configured to work with the five-wire mode by multiplexing clocks and frame-sync signals, if the ADCs and DAC are running at the same clock and sample rates.

Table 113: DSP Modes and Register Settings

I ² S Signal	Seven-Wire Mode	Five-Wire Mode (DAC)	Five-Wire Mode (ADC)	Top Level Wire
DAC Serial Clock	Available	Available	Same as ADC Serial Clock	RX_CLK
DAC Frame Sync	Available	Available	Same as ADC Frame Sync	RX_LRCK
DAC Serial DATA	Available	Available	Available	RX_DATA
ADC Serial Clock	Available	Same as DAC Serial Clock	Available	TX_CLK
ADC Frame Sync	Available	Same as DAC Frame Sync	Available	TX_LRCK
ADC Serial DATA1	Available	Available	Available	TX_DATA_1
ADC Serial DATA2	Available	Available	Available	TX_DATA_2

The following lists the two modes of DSP operation that Synaptics supports:

- Short frame sync mode
- Long frame sync mode

The PCM is supported in the DSP interface mode. The DSP mode can also be configured to drive/receive data and frame sync on the negative edge of the serial clock (see "[I2S_CLK_CTRL—0x0C](#)" on page 195).

DSP Short Frame Sync Mode

In DSP short frame sync mode, the falling edge of LRCK indicates the start of the DSP word. The LRCK is one clock long. Data is driven out on the rising edge of BCLK after the LRCK pulse.

To configure the CX20810/CX20811 DSP to the short frame sync normal mode, set I2S_DSP_SEL and DSP_DSTAT_DLY to HIGH. In the master DSP short frame sync mode, TX/RX_WS_WID is also set to 7'h00 along with DSP_DSTAT_DLY. The DSP_CTRL through DSP_RX_CTRL_1 registers are used to configure specific usage scenarios. The TX_WS_WID, RX_WS_WID, TX_FRM_LEN, and RX_FRM_LEN bits are used to describe the LRCK and frame length relation.

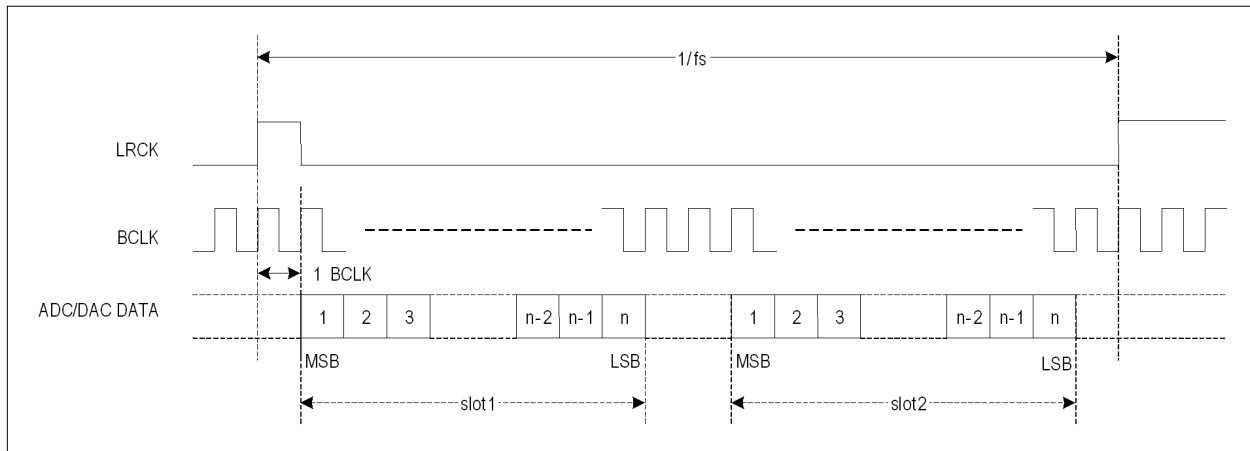


Figure 76: DSP Short Frame Sync Mode

DSP Short Frame Sync Mode—TDM Mode

In DSP short frame sync TDM mode, I2S_DSP_SEL and DSP_DSTAT_DLY are set HIGH. In the master DSP short frame sync TDM mode, TX/RX_WS_WID is also set to 7'h00 along with DSP_DSTAT_DLY. Set the DSP_TX_OUT_LINE_SEL and DSP_TX_TRI_N bits to HIGH. The DSP_CTRL through DSP_RX_CTRL_1 registers are used to configure specific usage scenarios. The TX_WS_WID, RX_WS_WID, TX_FRM_LEN, and RX_FRM_LEN bits are used to describe the LRCK and frame length relation.

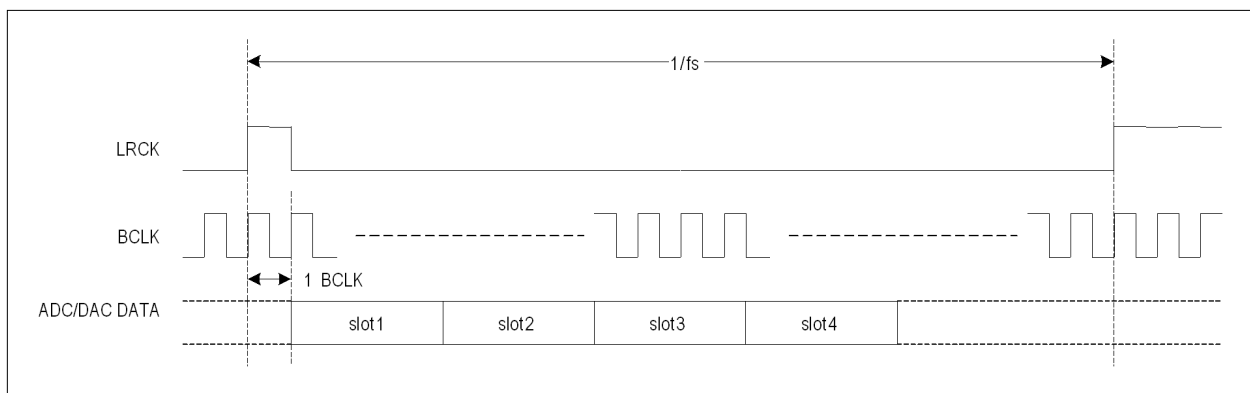


Figure 77: DSP Short Frame Sync in TDM Mode

Note: When channel slots are being programmed, slot values should be programmed so that $\text{ch-slot1} < \text{ch-slot2} < \text{ch-slot3} < \text{ch-slot4}$ (where $\text{ch-slot}/N$ represents the first slot number of channel N). If all four Tx channels are enabled, ch-slot4 should be the last channel in the frame. Similarly, if only three channels are enabled (using ch-slot1 , ch-slot2 , and ch-slot3), ch-slot3 should be the last channel in the frame. This is the default behavior, otherwise, the channel number with maximum $\text{ch-slot}/N$ value needs to be programmed in DSP_LAST_ADC_CH, and the DSP_LAST_ADC_CH_EN bit must be enabled.

DSP Long Frame Sync Mode

In DSP long frame sync mode, the rising edge of LRCK indicates the start of the DSP word. The LRCK is at least one Bclock long. Data is driven out on the rising edge of BCLK and synchronizes with the rising edge of LRCK.

Program the I2S_DSP_SEL to HIGH and DSP_DSTAT_DLY fields LOW to configure the CX20810/ CX20811 DSP to the long frame sync normal mode. The DSP_CTRL through DSP_RX_CTRL_1 registers are used to configure specific usage scenario. The TX_WS_WID, RX_WS_WID, TX_FRM_LEN, and RX_FRM_LEN bits are used to describe the LRCK and frame length relation.

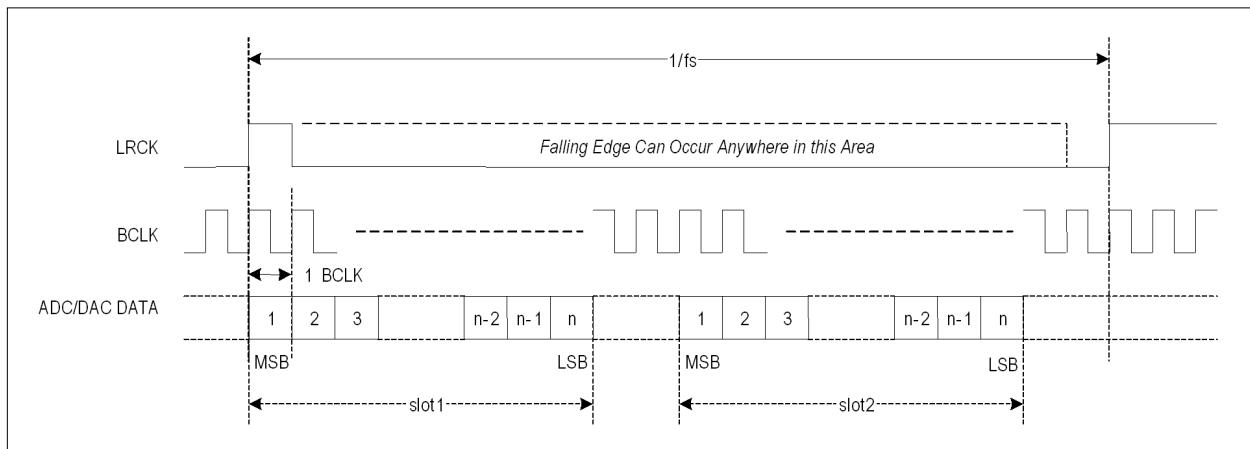


Figure 78: DSP Long Frame Sync Mode

DSP Long Frame Sync Mode—TDM Mode

In DSP long frame sync TDM mode, the DSP_TX_OUT_LINE_SEL and DSP_TX_TRI_N bits are set HIGH, I2S_DSP_SEL is set HIGH, and DSP_DSTAT_DLY is set to LOW. The DSP_CTRL through DSP_RX_CTRL_1 registers are used to configure specific usage scenarios.

The TX_WS_WID, RX_WS_WID, TX_FRM_LEN, and RX_FRM_LEN bits are used to describe the LRCK and frame length relation.

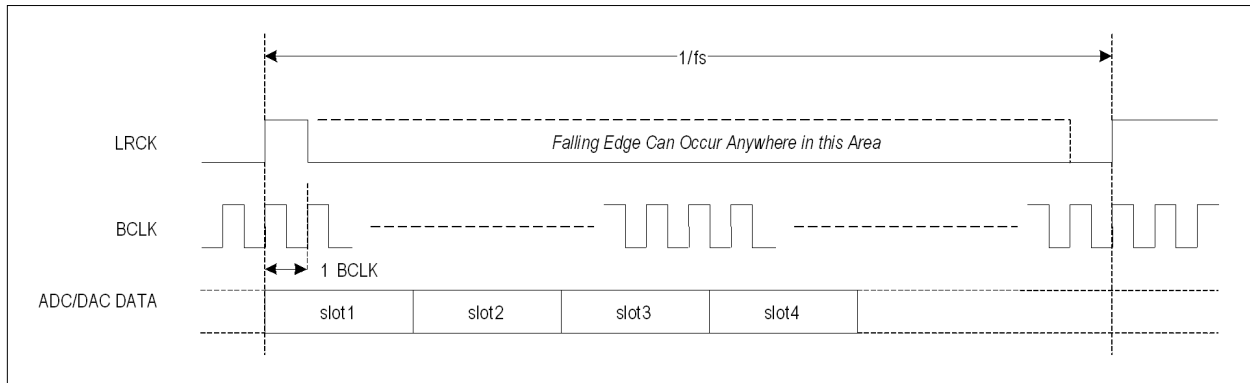


Figure 79: DSP Long Frame Sync in TDM Mode

The DSP can also be configured to work on the negative edge of BCLK (see "I2S_CLK_CTRL—0x0C" on page 195 and Figure 80 on page 162).

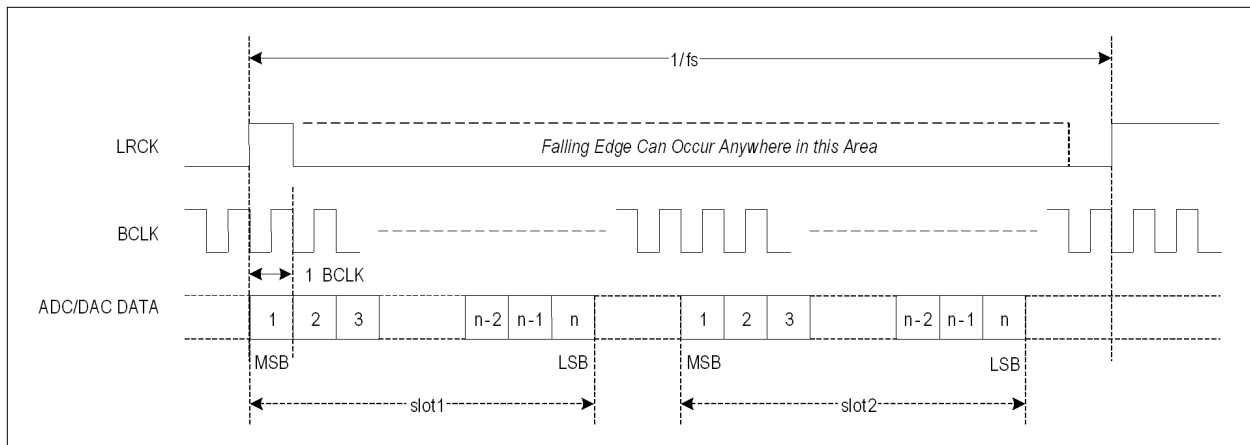


Figure 80: DSP Mode Running on the Negative Edge of BCLK

I2S/TDM Slave Mode

When the CX20810/CX20811 is configured as a bus slave device, it must accept incoming BCLK and LRCK signals and output ADC DATA (if the CX20811, also accept input DAC DATA).

Figure 81 shows one possible implementation where the bus master transitions LRCK synchronously with the BCLK's rising edge and the slave device outputs data also on BCLK's rising edge. In this case, the bus master expects the incoming ADC data to be settled and sampled on BCLK's falling edge. A one bit delay in the DATA stream is also shown below.

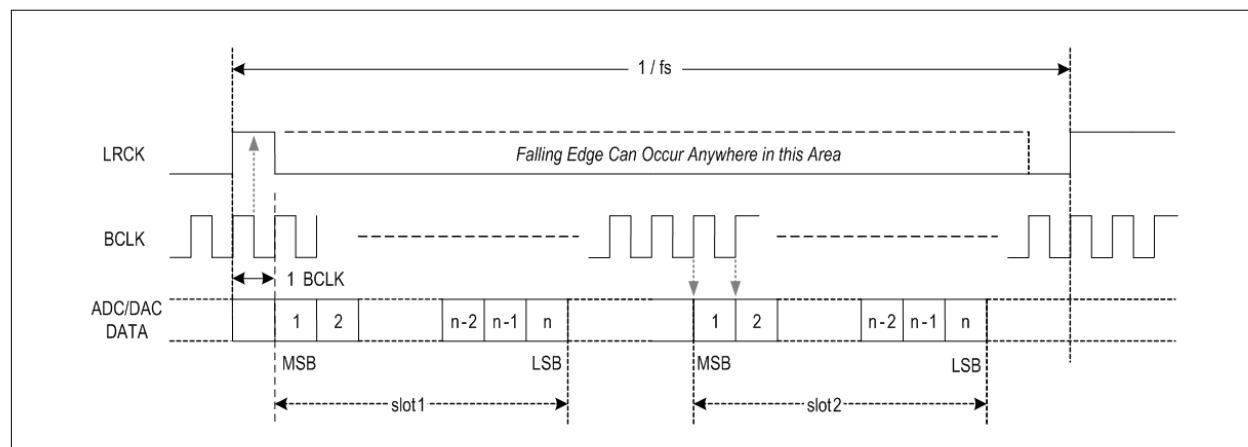


Figure 81: Slave Mode: Data Output Transitions on Rising Edge of BCLK

When configured as a slave device, the CX20810/CX20811 interface engine always samples LRCK on its clock's falling edge and transmits data on the same clock's rising edge. However register bit 0x0C [2] controls whether the logic block's clock is BCLK or an inverted version of BCLK. Thus, at a system level, the LRCK sampling and DATA transitioning can be inverted to suit the controller's needs.

The digital block's default behavior aligns with the intent shown in Figure 81. Register bit 0x0C [2] must therefore be set high so that the LRCK is sampled on the falling edge of BCLK and thus provides approximately a half-cycle of timing margin between frame detection and data transmission.

Figure 82 shows a more detailed diagram including the relevant internal signals (in blue):

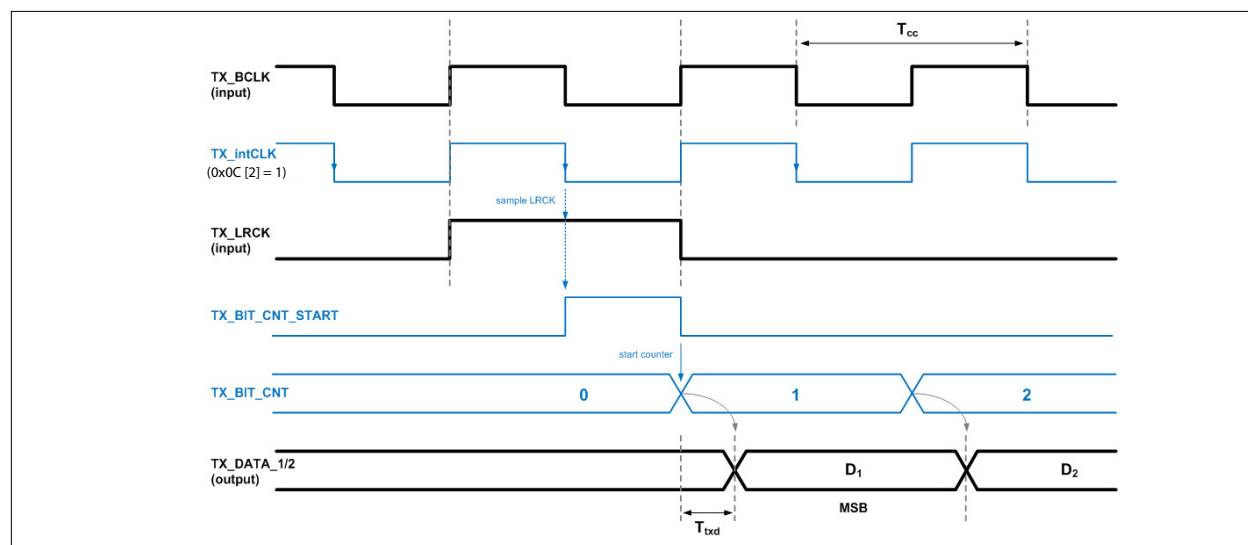


Figure 82: Detailed Timing: Slave Mode with DATA Transitions on Rising Edge of BCLK

- LRCK transitions on the rising edge of BCLK
- 0x0C [2] = 1: the internal logic clock TX_intCLK is a noninverted version of BCLK
- This internal clock samples LRCK on its falling edge.
- This produces a signal called BIT_CNT_START that is used to start the data bit counter
- On the rising edge of intCLK (rising edge of BCLK), data is transmitted out as the counter increments
- This arrangement results in a half-period of timing margin on the LRCK sampling

Alternatively, [Figure 83](#) shows the opposite case where LRCK and DATA transition on the falling edge of BCLK. LRCK now needs to be sampled on the rising edge of BCLK. This is opposite the edge setup within the logic block; therefore register bit 0x0C [2] must be set low to invert the BCLK internally.

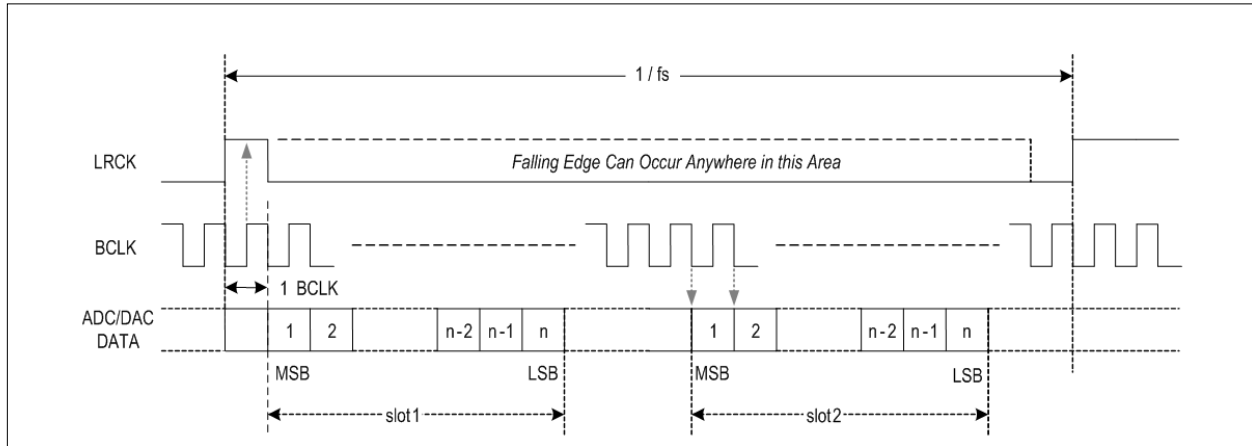


Figure 83: Slave Mode: Data Output Transitions on Falling Edge of BCLK

[Figure 84](#) provides a detailed diagram of this case:

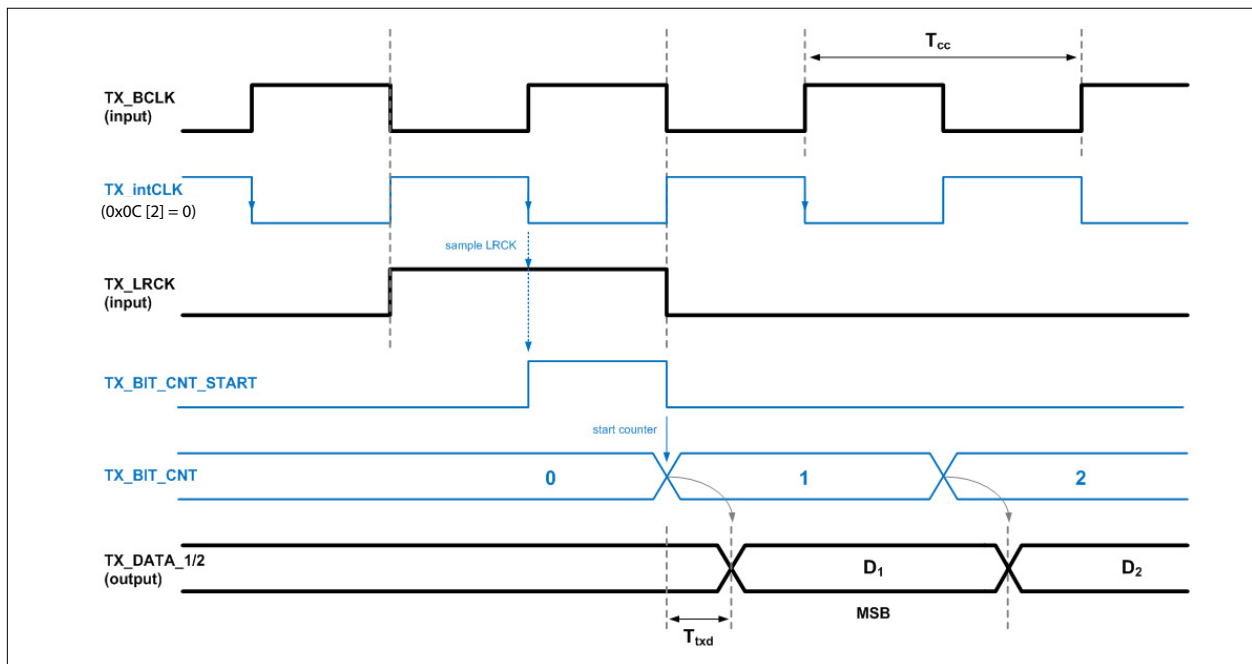


Figure 84: Detailed Timing: Slave Mode with Data Transitions on Falling Edge of BCLK

Recommended Register Settings

For slave mode operation, the following registers bits are key:

- Register bit 0x0C [2]: I2S_CLK_CTRL [2]: // DSP TX clock inversion control
- Register bit 0x35 [3]: I2S_TX_WSPOL: // LRCK channel select polarity control
- Register bit 0x39 [3]: DSP_DSTART_DLY: // DATA start delay control

In the case shown in [Figure 81 on page 163](#) (data launches on rising edge of BCLK with a 1-bit delay), the following register settings are required:

- Reg 0x0C = 0E // bit 2 = 1: internal clock is non-inverted version of BCLK
- Reg 0x35 = 00 // bit 3 = 0: normal LRCK channel select operation
- Reg 0x39 = 0A // bit 3 = 1: include 1-bit delay in DATA

For the case shown in [Figure 83 on page 164](#) (data launches on falling edge of BCLK with a 1-bit delay), the following registers settings are needed:

- Reg 0x0C = 0A // bit 2 = 0: internal clock is inverted version of BCLK
- Reg 0x35 = 00 // bit 3 = 0: normal LRCK channel select operation
- Reg 0x39 = 0A // bit 3 = 1: include 1-bit delay in DATA

Slave Mode Timing

[Figure 85](#) shows the detailed timing diagram and specifications.

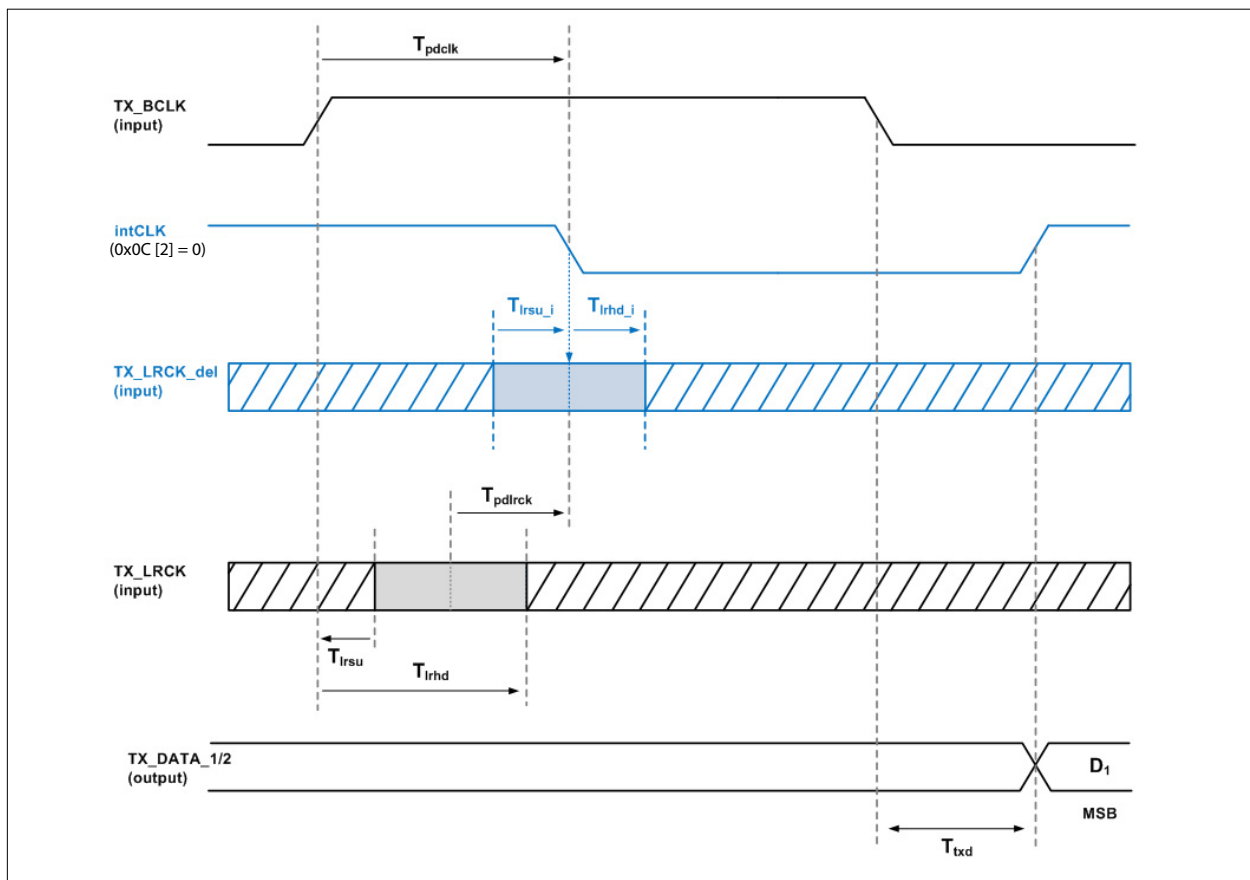


Figure 85: Slave Mode Timing Diagram: Data Transitions on Falling Edge of BCLK

- The BCLK and LRCK signals experience internal propagation delays due to pad and logic delays
- The internal logic setup and hold time requirements are less than 50 ps and are negligible relative to the propagation delay.
- Based on the worst case values, the minimum required setup time is -5 ns and minimum hold time is 7 ns. This is relative to the LRCK and BCLK signals seen at the device pins.
- Proper interface configuration will ensure around a half-cycle (~40 ns) of timing margin.

Table 114: Slave Mode Timing Specification

Parameter	Symbol	Min	Typ	Max	Unit
I2S/TDM bit clock cycle time	T _{CC}	80	81.38	–	ns
Internal propagation delay for TX_BCLK	T _{PDCLK}	10	–	12	ns
Internal propagation delay for TX_LRCK	T _{PDLRCK}	5	–	7	ns
TX_LRCK to TX_BCLK setup time	T _{LRSU}	-5	–	–	ns
TX_LRCK to TX_BCLK hold time	T _{LRHD}	+7	–	–	ns
TX Data propagation delay from falling edge of BCLK	T _{TXD}	5	–	20 *	ns

* Output delay assumes 3.3V IO and 30 pF load. For 1.8v IO and 20 pF load the max delay is 32 ns

System Integration

The CX20810/CX20811 digital audio interface can be connected to an external processor along with other CODECs in many ways. When the CX20810/CX20811 is connected to a processor as the only CODEC, normal modes can be chosen. This section shows the different modes of connecting CX20810/CX20811 with an external processor.

Normal Modes

- Figure 86 provides the seven-wire slave mode
- Figure 87 on page 167 provides the seven-wire master mode
- Figure 88 on page 168 provides the five-wire slave mode with DAC BCLK/LRCLK
- Figure 89 on page 168 provides the five-wire master mode with DAC BCLK/LRCLK
- Figure 90 on page 169 provides the five-wire slave mode with ADC BCLK/LRCLK
- Figure 91 on page 169 provides the five-wire master mode with ADC BCLK/LRCLK

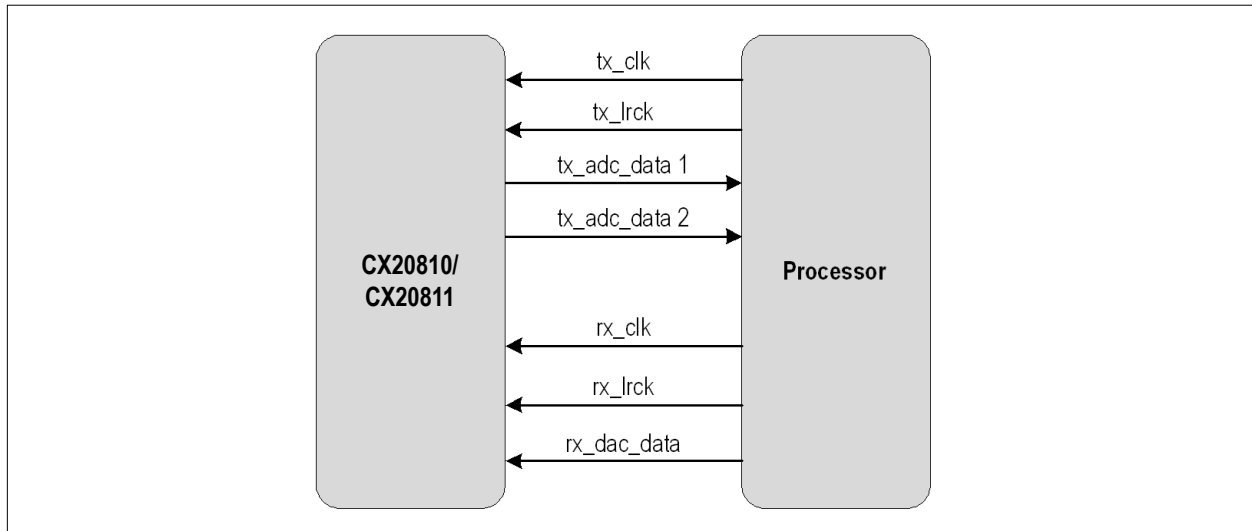


Figure 86: Seven-Wire Slave Mode

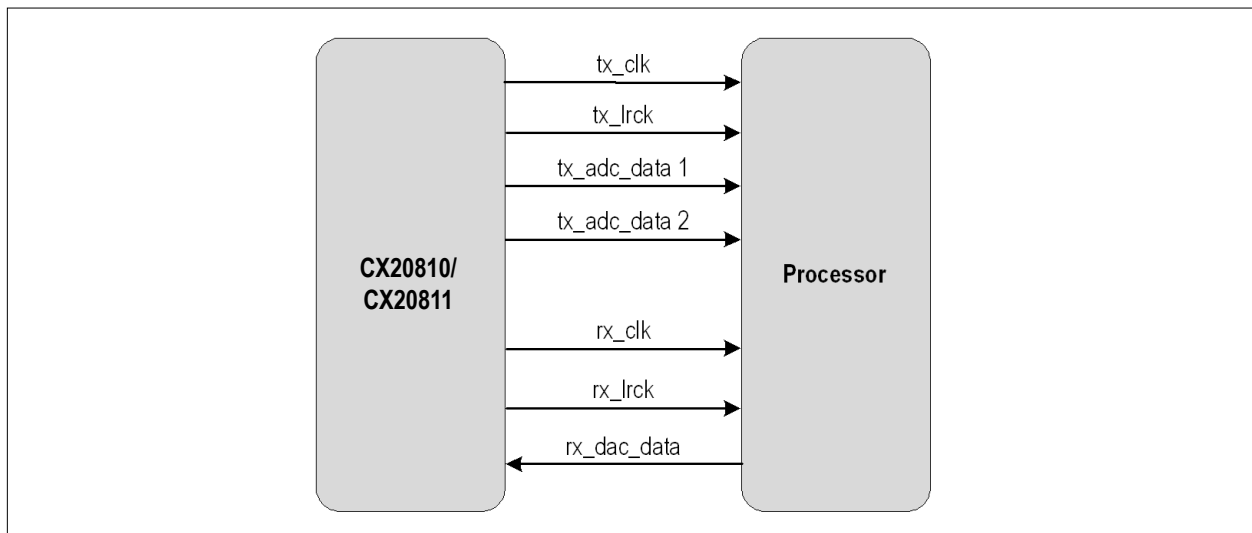


Figure 87: Seven-Wire Master Mode

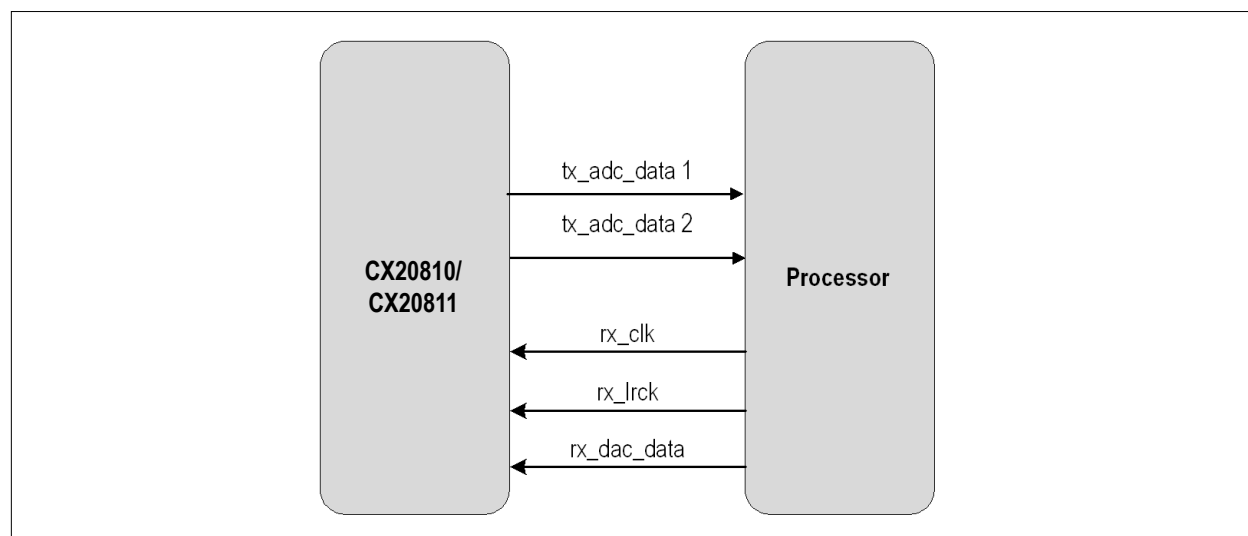


Figure 88: Five-Wire Slave Mode with DAC BCLK, LRCK

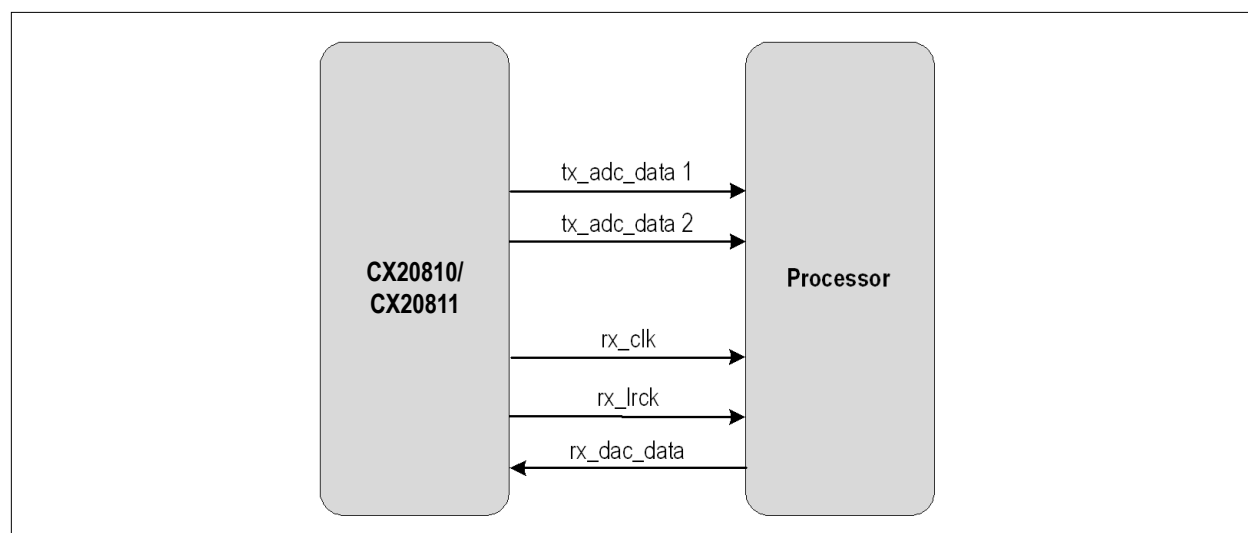


Figure 89: Five-Wire Master Mode with DAC BCLK, LRCK

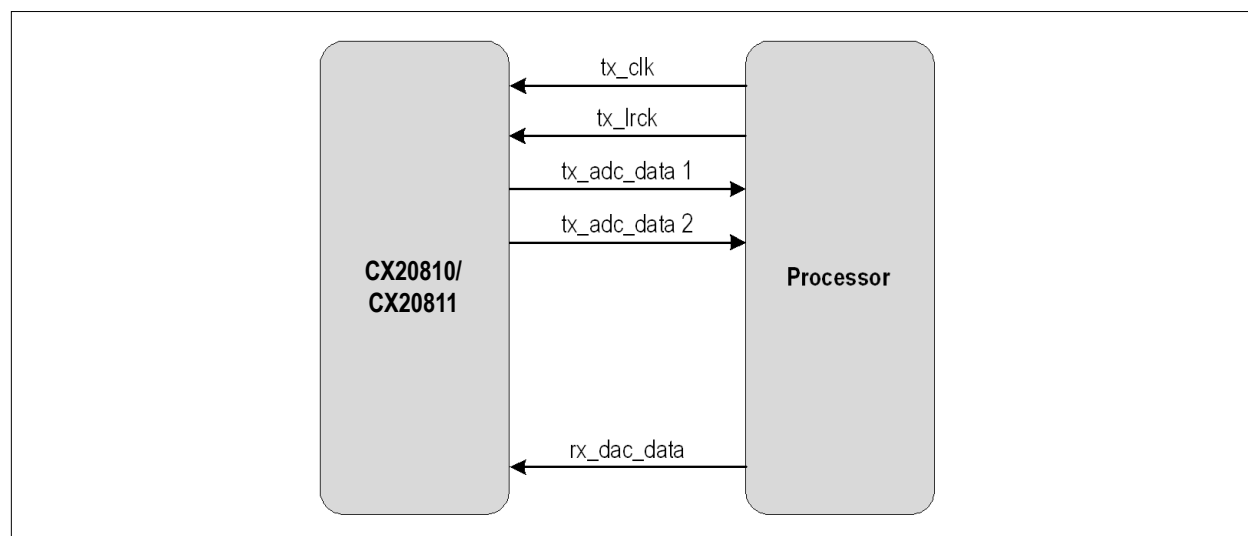


Figure 90: Five-Wire Slave Mode with ADC BCLK, LRCK

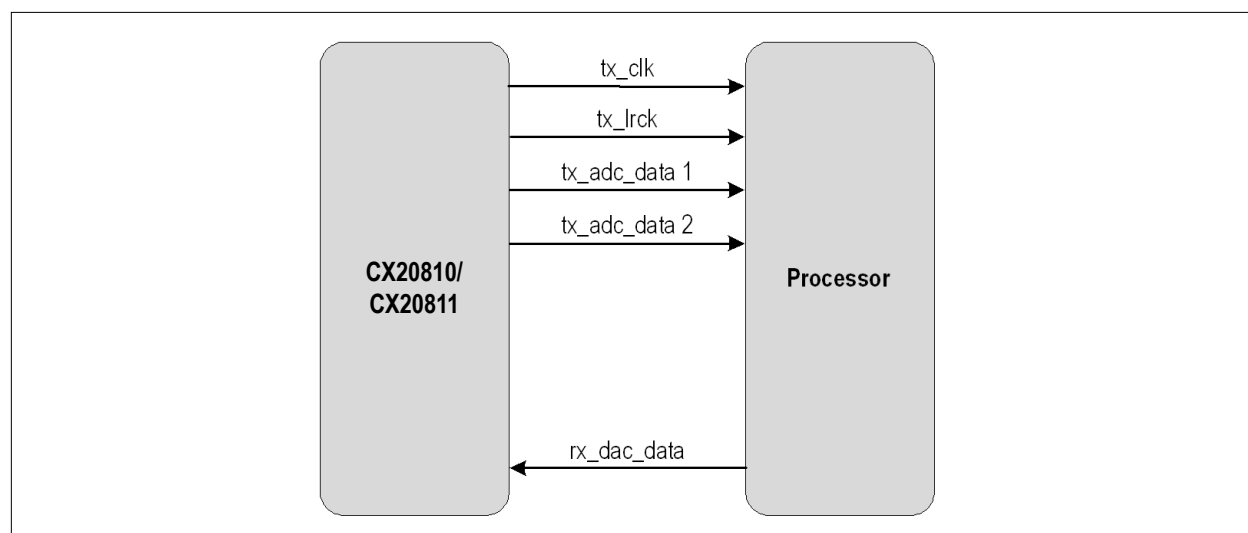


Figure 91: Five-Wire Master Mode with ADC BCLK, LRCK

TDM Modes

When multiple CX20810/CX20811 devices are connected to a processor or connected to a processor along with other CODECs, TDM modes are to be used.

- [Figure 92 on page 170](#) provides the TDM with CX20810/CX20811 as the master
- [Figure 93 on page 171](#) provides the TDM with other CODECs as the master
- [Figure 94 on page 172](#) provides the TDM with the processor as the master

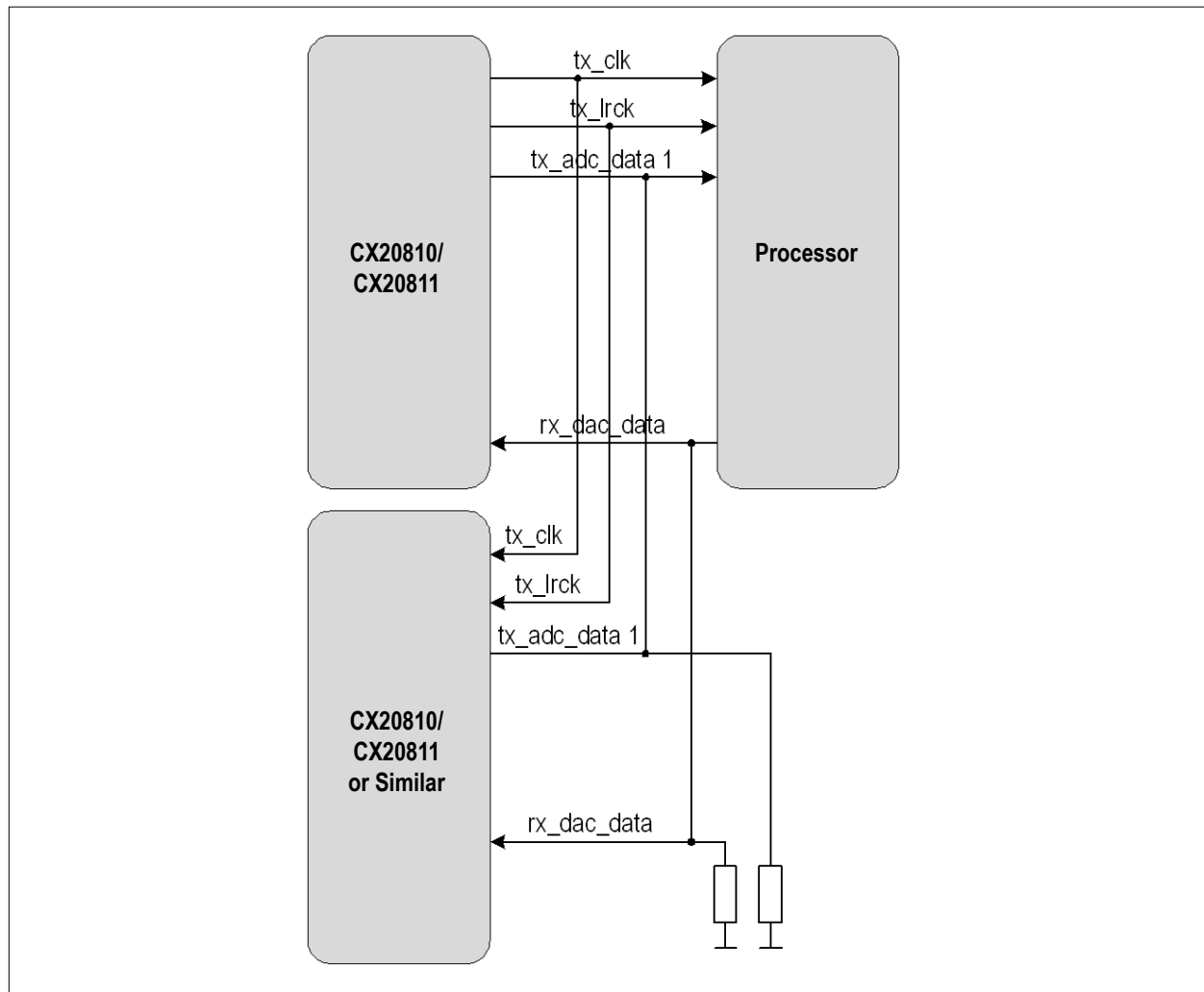


Figure 92: TDM with CX20810/CX20811 as the Master

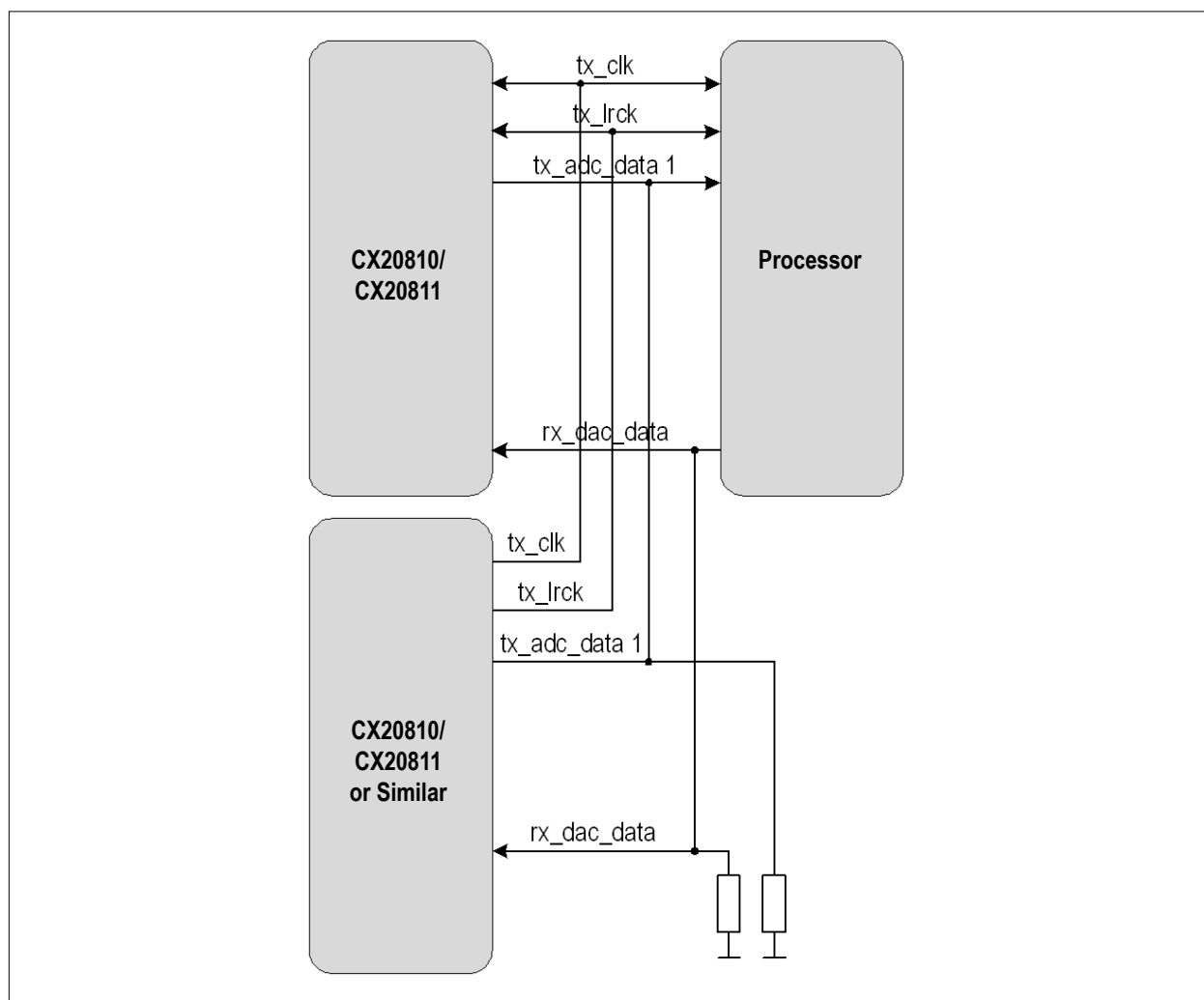


Figure 93: TDM with Other CODECs as the Master

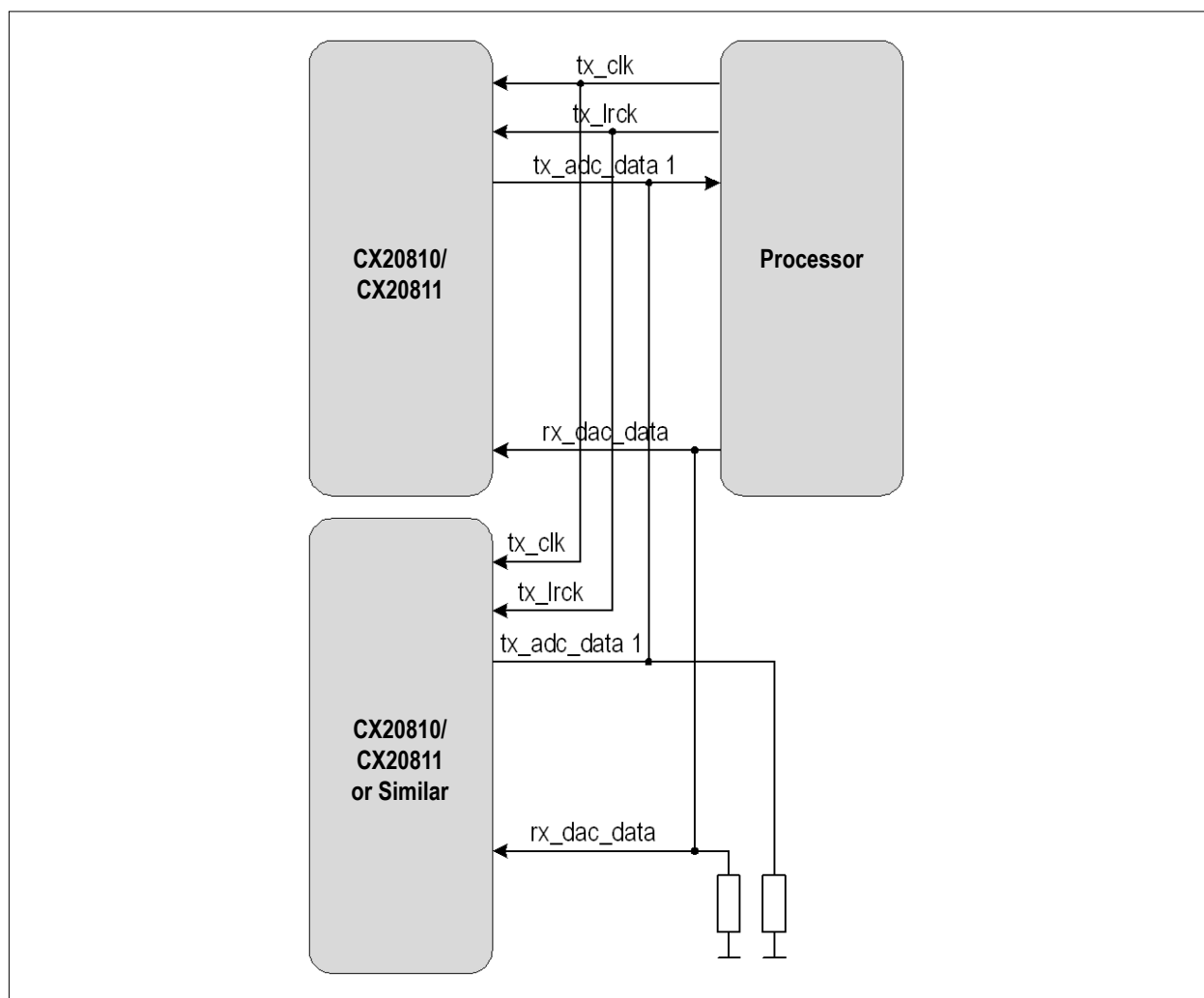


Figure 94: TDM with Processor as the Master

Eight-Channel TDM Usage Scenario

In TDM mode, the slots can be programmed to be four bytes wide to reflect the 32-bit mode. Because the CX20810/CX20811 is a 24-bit CODEC, the lower 8 bits are ignored on the Rx side and not driven on the Tx side.

In TDM mode, the CX20810/CX20811 can support an eight-channel 32-bit audio data interface up to a 48kHz sample rate.

Figure 94 on page 172 shows an example of an eight-channel, 32-bit implementation in which the CX20810/CX20811 can supply ADC data on any specific allotted slots. The unused slots can be shared by other CODECs.

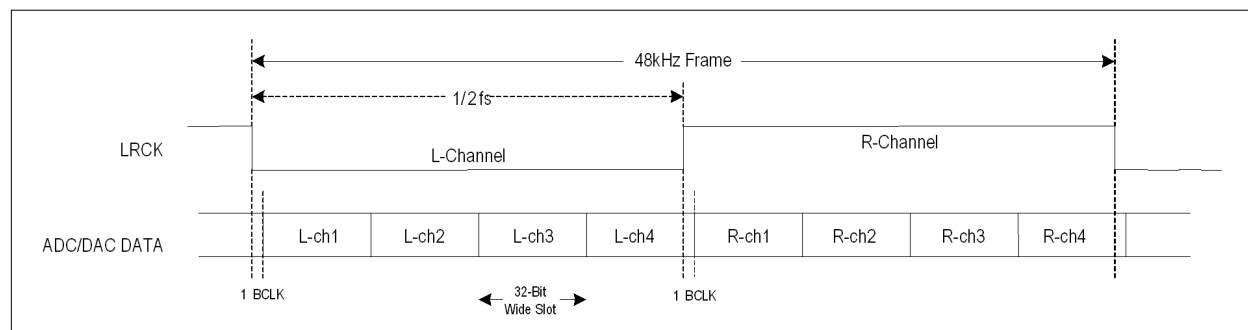


Figure 95: I²S TDM Mode Example Supporting Eight-Channel in 32-Bit Mode

Multi-Device Synchronization Using TDM Interface

Each CX20810/CX20811 device can support up to four ADC channels on the same I²S bus. A system that combines two or three devices together can provide eight or 12 channels of recording. All of the channels can then be transferred to the host processor on a single DATA line using the I²S TDM/PCM format. Figure 94 on page 172 shows an example where two CX2081X devices operate in slave mode and support 8 recording channels.

While each device is designed to operate its four channels synchronously, synchronization between devices requires specific initialization and sequencing to ensure that clocking on the two separate devices are in phase. Otherwise a sample clock phase shift may randomly be observed between devices. Figure 96 shows a block diagram of a single CX20810/CX20811 device.

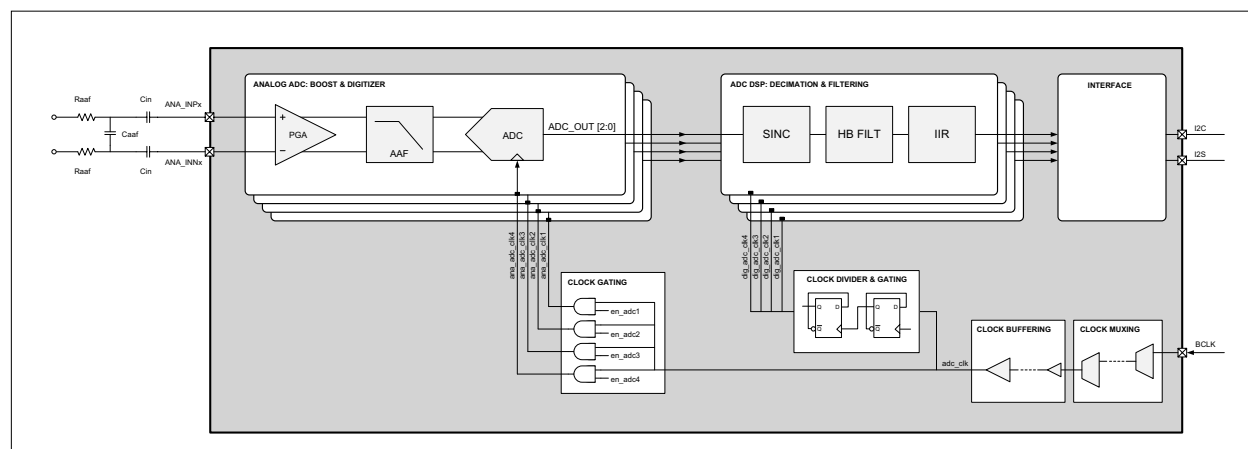


Figure 96: Single Device Recording Architecture

Assuming each CX20810/CX20811 device is configured as a digital interface slave and the on-chip PLL is bypassed, the incoming I²S clock (MCLK or BCLK depending on the configuration) generates a common clock defined as `adc_clk`. This single clock signal is applied to all four analog ADCs after passing through simple AND-based clock gating. The phase of the clocks driving the analog ADCs will therefore match the input I²S clock source. The `adc_clk` is also divided down to create the digital DSP clocks that clock the decimation and filtering circuitry. This is where the startup sequencing is required to properly initialize the clock dividers and ensure the digital ADC's clocks are in phase across multiple devices.

Synchronization Procedure

1. Disable the I²S clock.
2. Run the reset script on all slave devices. This applies a soft reset (register 0x0F) to all I²S digital logic and ADC DSP logic. By flushing the I²S FIFOs, it resets the FIFO read & write address pointers as well as resets the FIFO contents to 0x00.
3. Enable the I²S clock. This allows the main clock to propagate inside each device and reset the synchronous logic.
4. Disable the I²S clock.
5. Run the device configurations script on each device to setup the I²S format, ADCs, and any other blocks. Each slave devices will be fully configured before the system clock is applied to each device. Since there is no system clock, the clock dividers in each device will remain in their reset state (waiting for a clock edge) regardless of when each device is configured.
6. Enable the I²S clock. All slave devices will receive the same clock and all of their clock dividers will be operating on the same phase.

The preceding steps will remove any phase shifts due to digital clock misalignments. The remaining sources of phase error will contribute a very small amount of error. For example, the phase shift between a single device's channels due to variable clock delays through logic gates or on-chip routing should be minimal. If there were a 10 ns delta between channels (which is very large since we are concerned with the delta between the channel delays and not the absolute delays), that translates into a phase shift of less than 0.004 degrees at 1 kHz.

Similarly, clock skewing between two devices should also be minimal. Using 150 ps/inch as a rough estimate of PCB trace delay, there would need to be a very large routing imbalance for there to be a delay of any consequence.

Another source of recording phase error would be analog filter variation in the receive path. The external components provide a high pass and low pass function. Internally, there is additional low pass filtering due to the PGA and AAF circuitry. Simulations across PVT and component tolerances show that the worst-case phase shift between independent devices is 0.150 degrees at 1 kHz.

I²S Clocking

For certain sample rates in the audio interface master mode, the width of LRCK can be reduced so that no clocks per frame are without valid data on the data line. This process allows the same BW, but with slower clocks.

Example: Because the LRCK can be made 16 bits wide per channel in a 24kHz, 16-bit sample width mode, the frequency of BCLK required is $(24K * 16 * 2) = 768kHz$. The divider value to achieve 768kHz from 12.288MHz is 16 (I²S divider value = $(16 - 1) = 15$).

There are certain scenarios where it is not possible to derive the required BCLKs with 12.288MHz.

Example: In a 24kHz, 24-bit sample width mode, if LRCK is thought of being just 24 bits wide per channel, the required I²S clock is $(24K * 24 * 2) = 1.1152MHz$.

Because is not possible to achieve a 1.1152MHz clock from an integer divider with the 12.288MHz input, the next best LRCK width to achieve the highest possible BW in this case is 32 bits. With 32 bits wide LRCK per channel required, the I²S clock is $(24K * 32 * 2) = 1.536MHz$. The divider value to achieve 1.536MHz from 12.288MHz is 8 (I²S divider value = $(8 - 1) = 7$).

The following table provides the I²S divider values in various scenarios that are valid for the CX20810/CX20811.

Table 115: I²S Clocking Scenarios

Sample Rate (Hz)	Sample Bits Size	Minimum Clocks per Channel to Get Integer I ² S Divider Value	I ² S Clock Frequency (Hz)	I ² S Divider Value for 12.288MHz CLK
8000	8	8	128000	95
8000	16	16	256000	47
8000	24	24	384000	31
16000	8	8	256000	47
16000	16	16	512000	23
16000	24	24	768000	15
24000	8	8	384000	31
24000	16	16	768000	15
24000	24	32	1536000	7
32000	8	8	512000	23
32000	16	16	1024000	11
32000	24	24	1536000	7
48000	8	8	768000	15
48000	16	16	1536000	7
48000	24	32	3072000	3
96000	8	8	1536000	7
96000	16	16	3072000	3
96000	24	32	6144000	1

I²S Register Description

Table 116: I²S Register Description

Register Name	Register Address (Hex)	Default (Hex)
I2SDSP_CTRL_1	0x30	0x14
I2SDSP_CTRL_2	0x31	0x07
I2SDSP_CTRL_3	0x32	0x07
I2SDSP_MST_CTRL_1	0x33	0x1F
I2SDSP_MST_CTRL_2	0x34	0x1F
I2S_TX_CTRL_1	0x35	0x00
I2S_TX_CTRL_2	0x36	0x00
I2S_RX_CTRL_1	0x37	0x00
I2S_RX_CTRL_2	0x38	0x00
DSP_CTRL	0x39	0x00
DSP_TX_CTRL_1	0x3A	0x00
DSP_TX_CTRL_2	0x3B	0x00
DSP_TX_CTRL_3	0x3C	0x00
DSP_TX_CTRL_4	0x3D	0x00
DSP_TX_CTRL_5	0x3E	0x00
DSP_RX_CTRL_1	0x3F	0x00

I2SDSP_CTRL_1—0x30**Table 117:** I2SDSP_CTRL_1—0x30

Bits	Name	Default	R/W	Description
7	FIVE_WIRE_MODE	0	R/W	Sets the audio interface in five-wire mode: 0 = Seven-wire mode 1 = Five-wire mode In five-wire mode, the DAC bit clock and DAC LRCK are used for the ADC bit clock and ADC LRCK. The pins on the ADC bit clock and ADC LRCK are unused.
6	FIVE_CLK_LRCK	0	R/W	Selects whether the ADC or DAC control signals (CLK, LRCK) are used in five-wire mode: 0 = DAC CLK and LRCK used 1 = ADC CLK and LRCK used Note: Should be used only in five-wire mode.
5	Reserved	-	-	Reserved.
4:3	TX_SA_SIZE	0	R/W	Tx sample size control: 00 = 8-bit data 01 = 16-bit data 10 = 24-bit data 11 = Reserved
2:1	RX_SA_SIZE	0	R/W	Rx sample size control: 00 = 8-bit data 01 = 16-bit data 10 = 24-bit data 11 = Reserved
0	I2S_DSP_SEL	0	R/W	Mode select: 0 = Enables the normal mode in I²S, left-justified, and right-justified 1 = Enables the: - Normal mode in DSP - TDM mode in I²S, left-justified, right-justified and DSP

I2SDSP_CTRL_2—0x31**Table 118:** I2SDSP_CTRL_2—0x31

Bits	Name	Default	R/W	Description
7	LOOPBACK_ENABLE	0	R/W	Loopback enable bit, which is used as a test mode to loopback data from the DAC to ADC, or the ADC to DAC (see the LOOPBACK_TYPE field): 0 = Disables the loopback 1 = Enables the loopback Note: Loopback feature testing also needs proper setting of the LOOPBACK_MUX_SEL and LOOPBACK_TYPE fields.
6:5	LOOPBACK_MUX_SEL	0	R/W	Loopback ADC mux select: 00 = Selects the ADC1 channel for loopback 01 = Selects the ADC2 channel for loopback 10 = Selects the ADC3 channel for loopback 11 = Selects the ADC4 channel for loopback
4:0	TX_FRM_LEN	0	R/W	The Tx frame length in terms of bit clock cycles—it is $(N+1) * 8$: 00000 = 8 clocks per frame 00001 = 16 clocks per frame 00010 = 24 clocks per frame 00011 = 32 clocks per frame 11111 = 256 clocks per frame

I2SDSP_CTRL_3—0x32**Table 119:** I2SDSP_CTRL_3—0x32

Bits	Name	Default	R/W	Description
7	LOOPBACK_TYPE	0	R/W	Selects the type of loopback: 0 = DAC to ADC loopback 1 = ADC to DAC loopback
6:5	Reserved	-	-	Reserved.
4:0	RX_FRM_LEN	0	R/W	When in master mode, the Rx frame length in terms of bit clock cycles—it is $(N+1) * 8$ 00000 = 8 clocks per frame 00001 = 16 clocks per frame 00010 = 24 clocks per frame 00011 = 32 clocks per frame 11111 = 256 clocks per frame

I2SDSP_MST_CTRL_1—0x33**Table 120: I2SDSP_MST_CTRL_1—0x33**

Bits	Name	Default	R/W	Description
7	DSP_TDM_TX_CLK_INV	0	R/W	Inverts the Tx clock in the master mode of the DSP mode that runs on the negative edge of the clock and in the I2S_TDM mode: 0 = Do not invert the Tx clock (default) 1 = Invert the Tx clock Note: This bit should only be used in I2S_TDM and DSP modes that run on the negative edge of the Tx clock.
6:0	TX_WS_WID	0	R/W	When in master mode, the Tx WS (sync/LRCK) high phase width in terms of bit clock cycles: 0000000 = 1 cycle 0000001 = 2 cycle 1111111 = 128 cycles

I2SDSP_MST_CTRL_2—0x34**Table 121: I2SDSP_MST_CTRL_2—0x34**

Bits	Name	Default	R/W	Description
7	DSP_TDM_RX_CLK_INV	0	R/W	Inverts the Rx clock in the master mode of the DSP mode that runs on the negative edge of the clock and in the I2S_TDM mode: 0 = Do not invert the Rx clock (default) 1 = Invert the Rx clock Note: This bit should only be used in I2S_TDM and DSP modes that run on the negative edge of the Rx clock.
6:0	RX_WS_WID	0	R/W	When in master mode, the Rx WS (sync/LRCK) high phase width in terms of bit clock cycles: 0000000 = 1 cycle 0000001 = 2 cycle 1111111 = 128 cycles

I2S_TX_CTRL_1—0x35**Table 122: I2S_TX_CTRL_1—0x35**

Bits	Name	Default	R/W	Description
7	I2S1_TX_EN	0	R/W	Enables the I ² S-1 Tx when in I ² S, left-justified, and right-justified normal operation mode.
6	I2S1_TX_MUTE	0	R/W	Mutes the I ² S-1 Tx (all zeros are sent).
5	I2S2_TX_EN	0	R/W	Enables the I ² S-2 Tx when in I ² S, left-justified, and right-justified normal operation mode.
4	I2S2_TX_MUTE	0	R/W	Mutes the I ² S-2 Tx (all zeros are sent).
3	I2S_TX_WSPOL	0	R/W	A test mode control signal to invert the Tx (ADC) WS (LRCK) polarity: 0 = Polarity as per mode selected 1 = Invert polarity In: - I²S mode, the left channel data is on low WS - Left-justified mode and right-justified mode, the left channel data is on high WS If I2S_TX_WSPOL is set HIGH in: - I²S mode, the left channel data is on high WS - Left-justified and right-justified mode, the left channel data is on low WS
2:1	I2S_TX_MODE_SEL	0	R/W	Selects the mode for the Tx normal mode: 00 = I²S 01 = Left-justified 10 = Right-justified 11 = Reserved
0	Reserved	-	-	Reserved.

I2S_TX_CTRL_2—0x36**Table 123: I2S_TX_CTRL_2—0x36**

Bits	Name	Default	R/W	Description
7	Reserved	-	-	Reserved.
6:0	I2S_TX_BCNT_DLY	0	R/W	Only used in right-justified normal mode. If right-justified, this value indicates (N+1) delays in bit clock cycles for the first valid data transmitted: 7'h00 = 1 bit clock delay 7'h01 = 2 bit clock delay - Etc.

I2S_RX_CTRL_1—0x37**Table 124: I2S_RX_CTRL_1—0x37**

Bits	Name	Default	R/W	Description
7	I2S_RX_EN	0	R/W	Enables the Rx when in I ² S, left-justified, and right-justified normal operation mode.
6	I2S_RX_MUTE	0	R/W	Mutes the Rx (all zeros are sent) when in I ² S, left-justified, and right-justified normal mode.
5	I2S_RX_ORDER	0	R/W	I ² S, left-justified, and right-justified Rx data order: 0 = Processor sends data on the left channel 1 = Processor sends data on the right channel
4	Reserved	-	-	Reserved.
3	I2S_RX_WSPOL	0	R/W	A test mode control signal to invert the Rx (DAC) WS (LRCK) polarity: 0 = Polarity as per mode selected 1 = Invert polarity In: - I²S mode, the left channel data is on low WS - Left-justified mode and right-justified mode, the left channel data is on high WS If I2S_RX_WSPOL is set HIGH in: - I²S mode, the left channel data is on high WS - Left-justified and right-justified mode, the left channel data is on low WS
2:1	I2S_RX_MODE_SEL	0	R/W	Selects the mode for the Tx in normal mode: 00 = I²S 01 = Left-justified 10 = Right-justified 11 = Reserved
0	Reserved	-	-	Reserved.

I2S_RX_CTRL_2—0x38**Table 125: I2S_RX_CTRL_2—0x38**

Bits	Name	Default	R/W	Description
7	Reserved	-	-	Reserved.
6:0	I2S_RX_BCNT_DLY	0	R/W	Only used in right-justified normal mode. If right-justified, this value indicates (N+1) delays in the bit clock cycles for the first valid data transmitted: 7'h00 = 1 bit clock delay 7'h01 = 2 bit clock delay - Etc.

DSP_CTRL—0x39**Table 126: DSP_CTRL—0x39**

Bits	Name	Default	R/W	Description
7	DSP_TX_WSPOL	0	R/W	ADC LRCK inversion control: 0 = ADC LRCK is not inverted 1 = ADC LRCK is inverted This bit is only used in I ² S TDM modes.
6	DSP_RX_WSPOL	0	R/W	DAC LRCK inversion control: 0 = DAC LRCK is not inverted 1 = DAC LRCK is inverted This bit is only used in I ² S TDM modes.
5:4	Reserved	-	-	Reserved.
3	DSP_DSTART_DLY	0	R/W	DSP Tx and Rx data start delay control: 0 = Left-justified data is not delayed 1 = Left-justified data is delayed 1 bit Note: In DSP: - Slave short frame sync mode, DSP_DSTAT_DLY is set HIGH - Master short frame sync mode, set TX/RX_WS_WID to 7'h00 along with DSP_DSTAT_DLY This bit is also used in I ² S TDM mode.
2	DSP_DSHIFT_SEL	0	R/W	DSP Tx and Rx data shift select. Determines the data shift direction: 0 = MSB first 1 = LSB first
1	DSP_TX_OUT_LINE_SEL	0	R/W	0 = DSP sends ADC1, ADC2 data on sdata1 (tx_data_1) and ADC3, and ADC4 data on sdata2 (tx_data_2) 1 = DSP sends all four ADC data on sdata1(tx_data_1)
0	DSP_TX_TRI_N	0	R/W	Enables the DSP Tx output enable only for the slots that are actively supposed to drive: 0 = Tristate 1 = Do not tristate This bit is used in all the TDM modes.

DSP_TX_CTRL_1—0x3A**Table 127: DSP_TX_CTRL_1—0x3A**

Bits	Name	Default	R/W	Description
7:5	Reserved	-	-	Reserved.
4:0	DSP_TX_SLOT_1	0	R/W	First slot number for Tx channel 1. Each slot is 8 bits. All the enabled Tx channels should be configured with unique slot numbers. Note: If the Tx sample size is 16 or 24, it uses two or three consecutive slots respectively.

DSP_TX_CTRL_2—0x3B**Table 128: DSP_TX_CTRL_2—0x3B**

Bits	Name	Default	R/W	Description
7:5	Reserved	-	-	Reserved.
4:0	DSP_TX_SLOT_2	0	R/W	First slot number for Tx channel 2. Each slot is 8 bits. All the enabled Tx channels should be configured with unique slot numbers. Note: If the Tx sample size is 16 or 24, it uses two or three consecutive slots respectively.

DSP_TX_CTRL_3—0x3C**Table 129: DSP_TX_CTRL_3—0x3C**

Bits	Name	Default	R/W	Description
7:5	Reserved	-	-	Reserved.
4:0	DSP_TX_SLOT_3	0	R/W	First slot number for Tx channel 3. Each slot is 8 bits. All the enabled Tx channels should be configured with unique slot numbers. Note: If the Tx sample size is 16 or 24, it uses two or three consecutive slots respectively.

DSP_TX_CTRL_4—0x3D**Table 130: DSP_TX_CTRL_4—0x3D**

Bits	Name	Default	R/W	Description
7:5	Reserved	-	-	Reserved.
4:0	DSP_TX_SLOT_4	0	R/W	First slot number for Tx channel 4. Each slot is 8 bits. All the enabled Tx channels should be configured with unique slot numbers. Note: If the Tx sample size is 16 or 24, it uses two or three consecutive slots respectively.

DSP_TX_CTRL_5—0x3E**Table 131: DSP_TX_CTRL_5—0x3E**

Bits	Name	Default	R/W	Description
7	Reserved	-	-	Reserved.
6:5	DSP_LAST_ADC_CH	0	R/W	Channel number that represents the last channel in a frame: 0x0 = Channel 1 is the last channel in a frame 0x1 = Channel 2 is the last channel in a frame 0x2 = Channel 3 is the last channel in a frame 0x3 = Channel 4 is the last channel in a frame
4	DSP_LAST_ADC_CH_EN	0	R/W	Enable to use the last channel programmed in the DSP_LAST_ADC_CH field: 1 = Enable 0 = Disable (use the default) Note: This bit should be enabled only if the Tx channels are not in ascending order (i.e., tx_slot1 < tx_slot2 < tx_slot3 < tx_slot4).
3	DSP_TX_EN_4	0	R/W	Enables the Tx on channel 4 if the data interface is set to DSP normal operation mode or any TDM mode.
2	DSP_TX_EN_3	0	R/W	Enables the Tx on channel 3 if the data interface is set to DSP normal operation mode or any TDM mode.
1	DSP_TX_EN_2	0	R/W	Enables the Tx on channel 2 if the data interface is set to DSP normal operation mode or any TDM mode.
0	DSP_TX_EN_1	0	R/W	Enables the Tx on channel 1 if the data interface is set to DSP normal operation mode or any TDM mode.

DSP_RX_CTRL_1—0x3F**Table 132: DSP_RX_CTRL_1—0x3F**

Bits	Name	Default	R/W	Description
7	DSP_RX_EN	0	R/W	Enables the Rx on channel 1 in DSP normal operation mode or any TDM mode.
6:5	Reserved	-	-	Reserved.
4:0	DSP_RX_SLOT_1	0	R/W	First slot number for Rx channel 1. Each slot is 8 bits. Note: If the Rx sample size is 16 or 24, it uses two or three consecutive slots respectively.

Device Registers

Device Register Map

Table 133: Device Register Map

Register Name	Register Address (Hex)	Default (Hex)
PWR_CTRL_1	0x01	0x00
PWR_CTRL_2	0x02	0x00
PWR_CTRL_3	0x03	0x00
PWR_CTRL_4	0x04	0x00
PWR_CTRL_5	0x05	0x00
MCLK_CTRL	0x08	0x00
PLL_CLK_CTRL	0x09	0x00
I2S_TX_CLK_CTRL	0x0A	0x0B
I2S_RX_CLK_CTRL	0x0B	0x03
I2S_CLK_CTRL	0x0C	0x08
PLL_DIV_CTRL	0x0D	0x03
PWM_CLK_CTRL	0x0E	0x00
SOFT_RST_CTRL	0x0F	0x00
ADC_CLK_CTRL	0x10	0x00
ADC_EN_CTRL	0x11	0x10
ADC_OFFSET_CTRL0	0x12	0x00
ADC_OFFSET_CTRL1	0x13	0x00
MIXER_CTRL_0	0x14	0x00
MIXER_CTRL_1	0x15	0x00
ADC_TEST_CTRL0	0x16	0x55
ADC_MAP_CTRL1	0x17	0x00
ADC_TEST_CTRL2	0x18	0x00
ADC_TEST_CTRL3	0x19	0x00
ADC_TEST_CTRL4	0x1A	0x00
MIXER0_PGA	0x1B	0x11
MIXER1_PGA	0x1C	0x11
DSP_CLK_CTRL	0x1D	0x00
MIC_OFFSET_CLK_CTRL	0x1E	0x03
ADC1_PGA LSB	0x20	0x58
ADC1_PGA MSB	0x21	0x02
ADC2_PGA LSB	0x22	0x58
ADC2_PGA MSB	0x23	0x02
ADC3_PGA LSB	0x24	0x58
ADC3_PGA MSB	0x25	0x02
ADC4_PGA LSB	0x26	0x58
ADC4_PGA MSB	0x27	0x02

Table 133: Device Register Map (Continued)

Register Name	Register Address (Hex)	Default (Hex)
DAC_EN_GAIN	0x28	0x94
DAC_RATE_PWM	0x29	0x40
HP_FILT_PWN_EN	0x2A	0x00
DAC_CEN_CTRL	0x2B	0x00
EQ_COEFF_BIST_STATUS	0x2C	0x00
BIST_EN_MEM_STATUS	0x2D	0x00
ADC_MEM_STATUS	0x2E	0x00
DAC_POST_RAMP	0x2F	0x14
I2SDSP_CTRL_1	0x30	0x14
I2SDSP_CTRL_2	0x31	0x07
I2SDSP_CTRL_3	0x32	0x07
I2SDSP_MST_CTRL_1	0x33	0x1F
I2SDSP_MST_CTRL_2	0x34	0x1F
I2S_TX_CTRL_1	0x35	0x00
I2S_TX_CTRL_2	0x36	0x00
I2S_RX_CTRL_1	0x37	0x00
I2S_RX_CTRL_2	0x38	0x00
DSP_CTRL	0x39	0x00
DSP_TX_CTRL_1	0x3A	0x00
DSP_TX_CTRL_2	0x3B	0x00
DSP_TX_CTRL_3	0x3C	0x00
DSP_TX_CTRL_4	0x3D	0x00
DSP_TX_CTRL_5	0x3E	0x00
DSP_RX_CTRL_1	0x3F	0x00
FIFO_CTRL	0x40	0x00
DC_PROT_0	0x55	0x00
DC_PROT_1	0x56	0x00
PLL_CTRL_1	0x60	0x00
PLL_CTRL_2	0x61	0x00
PLL_CTRL_3	0x62	0x00
PLL_CTRL_4	0x63	0x00
PLL_CTRL_5	0x64	0x00
PLL_CTRL_6	0x65	0x00
PLL_CTRL_7	0x66	0x00
PLL_CTRL_8	0x67	0x00
PLL_CTRL_9	0x68	0x00
PLL_CTRL_10	0x69	0x00
PWM_CTRL_1	0x70	0x00
PWM_CTRL_2	0x71	0x00
PWM_CTRL_3	0x72	0x00

Table 133: Device Register Map (Continued)

Register Name	Register Address (Hex)	Default (Hex)
PWM_CTRL_4	0x73	0x00
PWM_CTRL_5	0x74	0x00
PWM_CTRL_6	0x75	0x00
REF_CTRL_1	0x78	0x00
REF_CTRL_2	0x79	0x00
REF_CTRL_3	0x7A	0x00
REF_CTRL_4	0x7B	0x00
ANA_CTRL_1	0x7C	0x00
ANA_CTRL_2	0x7D	0x00
MCLK_PAD_CTRL	0x80	0x02
I2S_PAD_CTRL	0x81	0x1C
I2S_RX_PAD_CTRL	0x82	0x2A
I2S_TX_PAD_CTRL	0x83	0xAA
GPIO0_PAD_CTRL	0x84	0x02
GPIO1_PAD_CTRL	0x85	0x02
GPIO2_PAD_CTRL	0x86	0x02
GPIO3_PAD_CTRL	0x87	0x02
GPIO_OUT	0x88	0x00
GPIO_IN	0x89	0x00
GPIO_INTR_CTRL	0x8A	0x00
GPIO_INTR_EN	0x8B	0x00
GPIO_INTR_STATUS	0x8C	0x00
WAKE_D2D_PAD_CTRL	0x8D	0x02
I2S_PAD_CTRL2	0x8E	0x1C
I2S_PAD_CTRL3	0x8F	0xFC
IIR_COEFF_B0_LOW	0x90	0x00
IIR_COEFF_B0_HIGH	0x91	0x00
IIR_COEFF_B1_LOW	0x92	0x00
IIR_COEFF_B1_HIGH	0x93	0x00
IIR_COEFF_B2_LOW	0x94	0x00
IIR_COEFF_B2_HIGH	0x95	0x00
IIR_COEFF_A1_LOW	0x96	0x00
IIR_COEFF_A1_HIGH	0x97	0x00
IIR_COEFF_A2_LOW	0x98	0x00
IIR_COEFF_A2_HIGH	0x99	0x00
COEFF_IIR_G	0x9A	0x00
IIR_EN	0x9B	0x00
COEFF_LATCH_EN	0x9C	0x00
ATT_SEL	0x9D	0x00
ANA_ADC1_CTRL_1	0xA0	0x00

Table 133: Device Register Map (Continued)

Register Name	Register Address (Hex)	Default (Hex)
ANA_ADC1_CTRL_2	0xA1	0x00
ANA_ADC1_CTRL_3	0xA2	0x00
ANA_ADC1_CTRL_4	0xA3	0x00
ANA_ADC1_CTRL_5	0xA4	0x00
ANA_ADC1_CTRL_6	0xA5	0x00
ANA_ADC1_CTRL_7	0xA6	0x00
ANA_ADC2_CTRL_1	0xA7	0x00
ANA_ADC2_CTRL_2	0xA8	0x00
ANA_ADC2_CTRL_3	0xA9	0x00
ANA_ADC2_CTRL_4	0xAA	0x00
ANA_ADC2_CTRL_5	0xAB	0x00
ANA_ADC2_CTRL_6	0xAC	0x00
ANA_ADC2_CTRL_7	0xAD	0x00
ANA_ADC3_CTRL_1	0xAE	0x00
ANA_ADC3_CTRL_2	0xAF	0x00
ANA_ADC3_CTRL_3	0xB0	0x00
ANA_ADC3_CTRL_4	0xB1	0x00
ANA_ADC3_CTRL_5	0xB2	0x00
ANA_ADC3_CTRL_6	0xB3	0x00
ANA_ADC3_CTRL_7	0xB4	0x00
ANA_ADC4_CTRL_1	0xB5	0x00
ANA_ADC4_CTRL_2	0xB6	0x00
ANA_ADC4_CTRL_3	0xB7	0x00
ANA_ADC4_CTRL_4	0xB8	0x00
ANA_ADC4_CTRL_5	0xB9	0x00
ANA_ADC4_CTRL_6	0xBA	0x00
ANA_ADC4_CTRL_7	0xBB	0x00
ADC1_ANALOG_PGA	0xBC	0x00
ADC2_ANALOG_PGA	0xBD	0x00
ADC3_ANALOG_PGA	0xBE	0x00
ADC4_ANALOG_PGA	0xBF	0x00
DTEST0	0xC0	0x00
DTEST1	0xC1	0x00
DTEST2	0xC2	0x00
CTEST0	0xD0	0x00
CTEST1	0xD1	0x00
CTEST2	0xD2	0x00
CTEST3	0xD3	0x00
CTEST4	0xD4	0x00
CTEST5	0xD5	0x00

Table 133: Device Register Map (Continued)

Register Name	Register Address (Hex)	Default (Hex)
CTEST6	0xD6	0x00
CTEST7	0xD7	0x00
CTEST8	0xD8	0x00
CTEST9	0xD9	0x00
CTEST10	0xDA	0x00
CTEST11	0xDB	0x00
CP_STATUS	0xE0	Reserved
PWM_STATUS	0xE1	Reserved
MIC1_OFFSET_LSB	0xE2	0x00
MIC1_OFFSET_MSB	0xE3	0x02
MIC2_OFFSET_LSB	0xE4	0x00
MIC2_OFFSET_MSB	0xE5	0x02
MIC3_OFFSET_LSB	0xE6	0x00
MIC3_OFFSET_MSB	0xE7	0x02
MIC4_OFFSET_LSB	0xE8	0x00
MIC4_OFFSET_MSB	0xE9	0x02
DEVICE_ID	0xFD, 0xFC	0x00, 0x51
BOND_PAD_STATUS	0xFF	0x00
REVISION ID/STEPPING ID	0xFE	0x00

Analog Power (PWR) Control Registers

PWR_CTRL_1—0x01

Table 134: PWR_CTRL_1—0x01

Bits	Name	Default	R/W	Description
7:4	CP12_CTRL [3:0]	0	R/W	CP output voltage programming: • 0 = 1.200V • 1 = 1.175V • 2 = 1.150V • 3 = 1.125V • 4 = 1.100V • 5 = 1.075V • 6 = 1.050V • 7 = 1.025V • 8 = 1.400V • 9 = 1.375V • 10 = 1.350V • 11 = 1.325V • 12 = 1.300V • 13 = 1.275V • 14 = 1.250V • 15 = 1.225V
3	CP12_SENSE_SELECT	0	R/W	CP feedback sensing mux: • 0 = vdd_core (normal behavior) • 1 = vdd_cp12out (test mode)
2:1	CP12_LOOPMODE [1:0]	0	R/W	CP operation mode control: • 0 = Normal (linear + skip) • 1 = Linear only • 2 = Skip only (do not use with 5V supply) • 3 = Disables the power stage and is put into a high-Z state (test mode only)
0	LDO18PLL_ENABLE	0	R/W	Enables the 1.8V LDO for PLL: • 0 = Disables the LDO • 1 = Enables the LDO

PWR_CTRL_2—0x02**Table 135: PWR_CTRL_2—0x02**

Bits	Name	Default	R/W	Description
7:6	CP12_SENSE_FILT [1:0]	0	R/W	CP sense-filter time constant: 0 = 2ns 1 = 150ns 2 = 300ns 3 = 600ns
5:4	CP12_FILT_SELW [1:0]	0	R/W	CP loop filter slew rate control: 0 = 51mV/μs 1 = 84mV/μs 2 = 26mV/μs 3 = 32mV/μs
3	CP12_COMP_FF_EN	0	R/W	CP sample and hold of the loop filter input: 0 = No sampling (normal) 1 = Use sampling and hold
2	CP12_FORCE_ENABLE	0	R/W	CP software enable: 0 = Enables the CP to use the CP12_EN pin 1 = Forces the CP on the via bit
1	CP12_FORCE_RSTB	0	R/W	CP POR detection on the 3.3V: 0 = Monitors the 3.3V supply on the LDO33DIG pin—resets and disables the CP if voltage is below 2.4V 1 = Disables the POR
0	CP12_CLKDET_BYPASS	0	R/W	Bypasses CP clock detection circuitry: 0 = Enables the clock detection 1 = Disables the clock detection

PWR_CTRL_3—0x03**Table 136: PWR_CTRL_3—0x03**

Bits	Name	Default	R/W	Description
7	LDO33DIG_DIS_ILIM	0	R/W	Disables the output current limiting for the digital LDO: 0 = Enables the 50mA current limit 1 = Disables the current limit
6:4	LDO33DIG_CTRL [2:0]	0	R/W	Control digital LDO output voltage: 0 = 3.31V 1 = 3.25V 2 = 3.19V 3 = 3.13V 4 = 3.55V 5 = 3.49V 6 = 3.43V 7 = 3.37V
3	LDO18PLL_DIS_ILIM	0	R/W	Disables the output current limiting for the PLL LDO: 0 = Enables the 50mA current limit 1 = Disables the current limit
2:0	LDO18PLL_CTRL [2:0]	0	R/W	Control 1.8V LDO output voltage: 0 = 1.80V 1 = 1.69V 2 = 1.58V 3 = 1.46V 4 = 2.25V 5 = 2.14V 6 = 2.03V 7 = 1.92V

PWR_CTRL_4—0x04**Table 137: PWR_CTRL_4—0x04**

Bits	Name	Default	R/W	Description
7:2	Reserved	0	R/W	Reserved.
1	PLL_DISABLE_DSMCLKOUT	0	R/W	Disables the PLL output to the analog core: 0 = Enables the PLL clock direct to the analog core 1 = Disables the clock
0	PLL_FORCE_POR18	0	R/W	Bypasses the 1.8V LDO state for the PLL output to the analog core: 0 = Enables the PLL output to the analog when the 1.8V LDO is enabled 1 = Enables the PLL output to the analog, independent of the 1.8V LDO state

PWR_CTRL_5—0x05*Table 138: PWR_CTRL_5—0x05*

Bits	Name	Default	R/W	Description
7:0	Reserved	0	-	Reserved.

MCLK_CTRL—0x08*Table 139: MCLK_CTRL—0x08*

Bits	Name	Default	R/W	Description
7	Reserved	0	-	Reserved.
6	MCLK_CTRL [6]	0	R/W	Clock to register the block to the latch status of the GPIO and so forth: 0 = CODEC_clk_d2d 1 = Reserved
5	MCLK_CTRL [5]	0	R/W	MCLK gate enable to the entire chip: 0 = Gates the clock 1 = Enables the clock
4	MCLK_CTRL [4]	0	R/W	0 = MCLK from the pin feeds the PLL 1 = MCLK from the programmable divider feeds the PLL
3	MCLK_CTRL [3]	0	R/W	Enable for the divisor change of MCLK. The programmable divider change is done through steps. Change the divisor value in MCLK_CTRL [2:0] and then set this bit = 0 → 1 to enable the divisor change.
2:0	MCLK_CTRL [2:0]	0	R/W	Divided version of MCLK (MCLK_CTRL [2:0] +1). The source clock is MCLK. The values are from 2–8. If programmed for value of 0 or 1, the divider output is MCLK/2.

PLL_CLK_CTRL—0x09**Table 140: PLL_CLK_CTRL—0x09**

Bits	Name	Default	R/W	Description
7:6	PLL_CLK_CTRL [7:6]	0	R/W	Selects MCLK or the bit clock from the external to feed the PLL: 00 = MCLK or divided version of MCLK 01 = I²S Tx bit clock 10 = I²S Rx bit clock 11 = GPIO3 (test mode using dtest4[3])
5:3	Reserved	0	-	Reserved.
2:1	PLL_CLK_CTRL [2:1]	0	R/W	Main clock for digital blocks: 00 = PLL 01 = MCLK or divided version of MCLK 10 = Reserved 11 = PLL divided version
0	PLL_CLK_CTRL [0]	0	R/W	Gates the main clock for the DSP. The clock selected by the mux select of PLL_CLK_CTRL [2:1] is gated: 0 = Gate for the DSP clocks and audio data interface clocks 1 = Clock enable for the DSP clocks and audio data interface clocks

I2S_TX_CLK_CTRL—0x0A**Table 141: I2S_TX_CLK_CTRL—0x0A**

Bits	Name	Default	R/W	Description
7	I2S_TX_CLK_CTRL [7]	0	R/W	Enable for the divisor change of I ² S/DSP Tx in master mode. First set the divisor value in I2S_TX_CLK_CTRL [6:0], and then set this bit to 1 to enable the divisor change.
6:0	I2S_TX_CLK_CTRL [6:0]	0x0B	R/W	I ² S/DSP Tx clock divide control source clk/ (I2S_TX_CLK_CTRL [6:0] + 1). The source clock can be PLL or MCLK based on the PLL_CLK_CTRL [2:1] register.

I2S_RX_CLK_CTRL—0x0B**Table 142: I2S_RX_CLK_CTRL—0x0B**

Bits	Name	Default	R/W	Description
7	I2S_RX_CLK_CTRL [7]	0	R/W	Enable for the divisor change of the I ² S/DSP Tx in master mode. First set the divisor value in I2S_RX_CLK_CTRL [6:0], and then set this bit to 1 to enable the divisor change.
6:0	I2S_RX_CLK_CTRL [6:0]	0x03	R/W	I ² S/DSP Rx clock divide control source clk/ (I2S_RX_CLK_CTRL [6:0] + 1). The source clock can be PLL or MCLK based on the PLL_CLK_CTRL [2:1] register.

I2S_CLK_CTRL—0x0C**Table 143: I2S_CLK_CTRL—0x0C**

Bits	Name	Default	R/W	Description
7	Reserved	0	-	Reserved.
6	I2S_CLK_CTRL [6]	0	R/W	Polarity of the I ² S/DSP Rx clock can be inverted: 0 = Default value 1 = Inverts the polarity Note: The Rx clock should be inverted in DSP Rx mode.
5	I2S_CLK_CTRL [5]	0	R/W	I ² S/DSP Rx clock gate enable: 0 = Gates the clock 1 = Enables the clock
4	I2S_CLK_CTRL [4]	0	R/W	Selects the I ² S/DSP Rx in master/slave mode: 0 = Slave mode 1 = Master mode
3	I2S_CLK_CTRL [3]	1	R/W	Clock gating for ADC3 and ADC4FIFOs in the I ² S/DSP module: 0 = Gates the clock to ADC3/4FIFOs 1 = Clock enable to ADC3/4FIFOs
2	I2S_CLK_CTRL [2]	0	R/W	Controls polarity of the internal clock applied to the interface engine (relative to BCLK) 0 = Internal clock is inverted version of BCLK 1 = Internal clock is non-inverted version of BCLK Note: In slave mode, LRCK is sampled on the clock edge that is opposite to the clock edge that launches DATA. Bit setting 0 is used when LRCK should be sampled on the rising edge of BCLK. Bit setting 1 is used when LRCK needs to be sampled on the falling edge of BCLK. See "I2S/TDM Slave Mode" on page 163 for more information.
1	I2S_CLK_CTRL [1]	0	R/W	I ² S/DSP Tx clock gate enable: 0 = Gates the clock 1 = Enables the clock
0	I2S_CLK_CTRL [0]	0	R/W	Selects the I ² S/DSP Tx in master/slave mode: 0 = Slave mode 1 = Master mode

PLL_DIV_CTRL—0x0D**Table 144: PLL_DIV_CTRL—0x0D**

Bits	Name	Default	R/W	Description
7:4	Reserved	0	-	Reserved.
3	PLL_DIV_CTRL [3]	0	R/W	PLL divider output gate enable to the entire chip: 0 = Gates the clock 1 = Enables the clock
2	PLL_DIV_CTRL [2]	0	R/W	Enable for the divisor change of the PLL divider. The programmable divider change is done through steps. Change the divisor value in [1:0] and then set this to 1 to enable the divisor change.
1:0	PLL_DIV_CTRL [1:0]	3	R/W	Divided version of the audio PLL (PLL_DIV_CTRL [1:0] +1). The source clock is audio PLL. Divide values of 2, 3, or 4 are available: 00b = pll_clk/2 (/1 is not available) 01b = pll_clk/2 10b = pll_clk/3 11b = pll_clk/4 See Table 140 on page 194 to bypass this divider if desired.

PWM_CLK_CTRL—0x0E**Table 145: PWM_CLK_CTRL—0x0E**

Bits	Name	Default	R/W	Description
7:4	Reserved	-	-	Reserved.
3	PWM_CLK_CTRL[3]	0	R/W	Clock gate for the DC detection counter: 0 = Gated 1 = Enables the clock for the DC detection counter
2	PWM_CLK_CTRL[2]	0	R/W	Clock gating for the dc_det filter: 0 = Gated 1 = Enables the clock
1	PWM_CLK_CTRL[1]	0	R/W	Clock gating for the PWM clock out to the analog PWM driver: 0 = Gated 1 = Enables the clock
0	PWM_CLK_CTRL[0]	0	R/W	Clock gating for the DAC/PWM digital engine: 0 = Gated 1 = Enables the clock

Note: For DC detection, enable both [3:2] bits.

SOFT_RST_CTRL—0x0F**Table 146:** *SOFT_RST_CTRL—0x0F*

Bits	Name	Default	R/W	Description
7:2	Reserved	-	-	Reserved.
1	SOFT_RST_CTRL[1]	0	R/W	When set to 1, sets all the values in the registers to their default values.
0	SOFT_RST_CTRL[0]	0	R/W	When set to 1, clears all the DSP and audio data interface values.

ADC, Mixer Registers

ADC_CLK_CTRL—0x10

Table 147: ADC_CLK_CTRL—0x10

Bits	Name	Default	R/W	Description
7	MIC_OFFSET_CLK_EN	0	R/W	Microphone offset calibration clock enable: 0 = Disables the clock for ADC offset calibration 1 = Enables the clock for ADC offset calibration
6	ADC_CLK_GATE_EN	0	R/W	Analog microphone clock gate enable: 0 = Disables the analog clock for ADC channel 1 = Enables the analog clock to ADC channel
5	ADC_CLK_SELECT	0	R/W	Analog microphone clock select: 0 = Sets the analog microphone clock to 12.288MHz 1 = Sets the analog microphone clock to 6.144MHz
4	ADC_CLK_CH4_EN	0	R/W	Clock gate enable for ADC4: 0 = Disables the clock to ADC channel 4 1 = Enables the clock to ADC channel 4
3	ADC_CLK_CH3_EN	0	R/W	Clock gate enable for ADC3: 0 = Disables the clock to ADC channel 3 1 = Enables the clock to ADC channel 3
2	ADC_CLK_CH2_EN	0	R/W	Clock gate enable for ADC2: 0 = Disables the clock to ADC channel 2 1 = Enables the clock to ADC channel 2
1	ADC_CLK_CH1_EN	0	R/W	Clock gate enable for ADC1: 0 = Disables the clock to ADC channel 1 1 = Enables the clock to ADC channel 1
0	ADC_CLK_ALL_EN	0	R/W	Clock gate enable for ADC digital: 0 = Disables the clock to all ADC channels 1 = Enables the clock to all ADC channels

ADC_EN_CTRL—0x11**Table 148: ADC_EN_CTRL—0x11**

Bits	Name	Default	R/W	Description
7	MIXER EN	0	R/W	When set, enables the mixer block based on how the ADC mapping mixer output is routed: 0 = Disables the mixer 1 = Enables the mixer
6:4	ADC_SAMPLE_RATE[2:0]	0	R/W	Sets the sample rate for all ADC channels: 0 = 8kHz 1 = 16kHz 2 = 24kHz/22.05kHz based on the PLL or external MCLK 3 = 32kHz 4 = 48kHz/44.1kHz based on the PLL or external MCLK 5 = 96kHz/88.2kHz based on the PLL or external MCLK 6 = Reserved 7 = Reserved
3	ADC_EN_CTRL[3]	0	R/W	Enable for ADC4: 0 = Disables ADC channel 4 1 = Enables ADC channel 4
2	ADC_EN_CTRL[2]	0	R/W	Enable for ADC3: 0 = Disables ADC channel 3 1 = Enables ADC channel 3
1	ADC_EN_CTRL[1]	0	R/W	Enable for ADC2: 0 = Disables ADC channel 2 1 = Enables ADC channel 2
0	ADC_EN_CTRL[0]	0	R/W	Enable for ADC1: 0 = Disables ADC channel 1 1 = Enables ADC channel 1

ADC_OFFSET_CTRL0—0x12**Table 149: ADC_OFFSET_CTRL0—0x12**

Bits	Name	Default	R/W	Description
7:4	Reserved	0	-	Reserved.
3	MIC_OFFSET_CAL_EN4	0	R/W	Enables channel 4's SAR engine for one-time calibration: 0 = Disables the offset calibration engine 1 = Enables the calibration engine
2	MIC_OFFSET_CAL_EN3	0	R/W	Enables channel 3's SAR engine for one-time calibration: 0 = Disables the offset calibration engine 1 = Enables the calibration engine
1	MIC_OFFSET_CAL_EN2	0	R/W	Enables channel 2's SAR engine for one-time calibration: 0 = Disables the offset calibration engine 1 = Enables the calibration engine
0	MIC_OFFSET_CAL_EN1	0	R/W	Enables channel 1's SAR engine for one-time calibration: 0 = Disables the offset calibration engine 1 = Enables the calibration engine

ADC_OFFSET_CTRL1—0x13**Table 150: ADC_OFFSET_CTRL1—0x13**

Bits	Name	Default	R/W	Description
7:3	MIC_OFFSET_CAL_GAIN [4:0]	0	R/W	Gain setting for which the calibration is done on the channel set by MIC_OFFSET_CAL_CHANNEL, if MIC_OFFSET_CAL_EN_SINGLE = 1.
2:1	MIC_OFFSET_CAL_CHANNEL	0	R/W	Selects the channel for which the particular gain set by MIC_OFFSET_CAL_GAIN[4:0] needs to be applied: 0 = Channel 1 1 = Channel 2 2 = Channel 3 3 = Channel 4
0	MIC_OFFSET_CAL_EN_SINGLE	0	R/W	Enables the calibration for the single gain programmed by MIC_OFFSET_CAL_GAIN[4:0]: 0 = No calibration 1 = Calibrate one-time for the gain programmed

MIXER_CTRL_0—0x14**Table 151:** *MIXER_CTRL_0—0x14*

Bits	Name	Default	R/W	Description
7:5	MIXER_CTRL0 [7:5]	0	R/W	Selects the mixer mode for ADC2: • 000 = Sum of the left channels (adc1+adc3) • 001 = Sum of the right channels (adc2+adc4) • 010 = Sum of the left and right channels (adc1+adc2) • 011 = Sum of the left and right channels (adc3+adc4) • 100 = Sum of all channels
4:2	MIXER_CTRL0 [4:2]	0	R/W	Selects the mixer mode for ADC1: • 000 = Sum of the left channels (adc1+adc3) • 001 = Sum of the right channels (adc2+adc4) • 010 = Sum of the left and right channels (adc1+adc2) • 011 = Sum of the left and right channels (adc3+adc4) • 100 = Sum of all channels
1	MIXER_CTRL0 [1]	0	R/W	Selects the mixer output on the ADC2 channel: • 0 = No operation (the mixer block, even if enabled, does not interfere in the normal microphone path) • 1 = Mixer output on ADC 2
0	MIXER_CTRL0 [0]	0	R/W	Selects the mixer output on the ADC1 channel: • 0 = No operation (the mixer block, even if enabled, does not interfere in the normal microphone path) • 1 = Mixer output on ADC 1

MIXER_CTRL_1—0x15**Table 152:** *MIXER_CTRL_1—0x15*

Bits	Name	Default	R/W	Description
7:5	MIXER_CTRL1 [7:5]	0	R/W	Selects the mixer mode for ADC4: • 000 = Sum of the left channels (adc1+adc3) • 001 = Sum of the right channels (adc2+adc4) • 010 = Sum of the left and right channels (adc1+adc2) • 011 = Sum of the left and right channels (adc3+adc4) • 100 = Sum of all channels
4:2	MIXER_CTRL1 [4:2]	0	R/W	Selects the mixer mode for ADC3: • 000 = Sum of the left channels (adc1+adc3) • 001 = Sum of the right channels (adc2+adc4) • 010 = Sum of the left and right channels (adc1+adc2) • 011 = Sum of the left and right channels (adc3+adc4) • 100 = Sum of all channels
1	MIXER_CTRL1 [1]	0	R/W	Selects the mixer output on the ADC4 channel: • 0 = No operation (the mixer block, even if enabled, does not interfere in the normal microphone path) • 1 = Mixer output on ADC4
0	MIXER_CTRL1 [0]	0	R/W	Selects the mixer output on the ADC3 channel: • 0 = No operation (the mixer block, even if enabled, does not interfere in the normal microphone path) • 1 = Mixer output on ADC3

ADC_TEST_CTRL0—0x16**Table 153: ADC_TEST_CTRL0—0x16**

Bits	Name	Default	R/W	Description
7	ADC_TEST_CTRL0 [7]	0	R/W	ADC channel 4 single bit mode: 0 = 3-bit analog interface 1 = Single bit interface as test
6	ADC_TEST_CTRL0 [6]	1	R/W	Bypasses the DC filter for ADC channel 4: 0 = No bypass 1 = Bypass
5	ADC_TEST_CTRL0 [5]	0	R/W	ADC channel 3 single bit mode: 0 = 3-bit analog interface 1 = Single bit interface as a test
4	ADC_TEST_CTRL0 [4]	1	R/W	Bypasses the DC filter for ADC channel 3: 0 = No bypass 1 = Bypass
3	ADC_TEST_CTRL0 [3]	0	R/W	ADC channel 2 single bit mode: 0 = 3-bit analog interface 1 = Single bit interface as a test
2	ADC_TEST_CTRL0 [2]	1	R/W	Bypasses the DC filter for ADC channel 2: 0 = No bypass 1 = Bypass
1	ADC_TEST_CTRL0 [1]	0	R/W	ADC channel 1 single bit mode: 0 = 3-bit analog interface 1 = Single bit interface as a test
0	ADC_TEST_CTRL0 [0]	1	R/W	Bypasses the DC filter for ADC channel 1: 0 = No bypass 1 = Bypass

ADC_MAP_CTRL1—0x17**Table 154:** ADC_MAP_CTRL1—0x17

Bits	Name	Default	R/W	Description
7:6	ADC_MAP_CTRL1 [7:6]	0	R/W	Maps that the analog microphone input is connected to for digital ADC4: 00 = Analog Mic4 01 = Analog Mic1 10 = Analog Mic2 11 = Analog Mic3
5:4	ADC_MAP_CTRL1 [5:4]	0	R/W	Maps that the analog microphone input is connected to for digital ADC3: 00 = Analog Mic3 01 = Analog Mic4 10 = Analog Mic1 11 = Analog Mic2
3:2	ADC_MAP_CTRL1 [3:2]	0	R/W	Maps that the analog microphone input is connected to for digital ADC2: 00 = Analog Mic2 01 = Analog Mic3 10 = Analog Mic4 11 = Analog Mic1
1:0	ADC_MAP_CTRL1 [1:0]	0	R/W	Maps that the analog microphone input is connected to for digital ADC1: 00 = Analog Mic1 01 = Analog Mic2 10 = Analog Mic3 11 = Analog Mic4

ADC_TEST_CTRL2—0x18**Table 155: ADC_TEST_CTRL2—0x18**

Bits	Name	Default	R/W	Description
7	ADC_TEST_CTRL2[7]	0	R/W	Bypasses the ADC4 analog gain compensation: 0 = Applies gain compensation 1 = No gain compensation
6	ADC_TEST_CTRL2[6]	0	R/W	Bypasses the ADC3 analog gain compensation: 0 = Applies gain compensation 1 = No gain compensation
5	ADC_TEST_CTRL2[5]	0	R/W	Bypasses the ADC2 analog gain compensation: 0 = Applies gain compensation 1 = No gain compensation
4	ADC_TEST_CTRL2[4]	0	R/W	Bypasses the ADC1 analog gain compensation: 0 = Applies gain compensation 1 = No gain compensation
3	ADC_TEST_CTRL2[3]	0	R/W	ADC4 block data is similar to mute or the secure microphone. For mute, use the PGA to slowly ramp-down the gain.
2	ADC_TEST_CTRL2[2]	0	R/W	ADC3 block data is similar to mute or the secure microphone. For mute, use the PGA to slowly ramp-down the gain.
1	ADC_TEST_CTRL2[1]	0	R/W	ADC2 block data is similar to mute or the secure microphone. For mute, use the PGA to slowly ramp-down the gain.
0	ADC_TEST_CTRL2[0]	0	R/W	ADC1 block data is similar to mute or the secure microphone. For mute, use the PGA to slowly ramp-down the gain.

ADC_TEST_CTRL3—0x19**Table 156: ADC_TEST_CTRL3—0x19**

Bits	Name	Default	R/W	Description
7	ADC_TEST_CTRL3 [7]	0	R/W	Enables loopback from the DAC FIFO to the ADC4 IIR input. Because the adc4 decimator out write signal is read for the DAC FIFO in this test mode, adc4 must be enabled to test any of the ADC IIR and other test signals are used to bypass the decimator out with interpolator in for the IIR: 0 = adc4_iir_in is output from the decimator 1 = adc4_iir_in is the DAC FIFO output
6	ADC_TEST_CTRL3 [6]	0	R/W	Enables loopback from the DAC FIFO to the ADC3 IIR input. Because the adc3 decimator out write signal is read for the DAC FIFO in this test mode, adc3 must be enabled to test any of the ADC IIR and other test signals are used to bypass the decimator out with interpolator in for the IIR: 0 = adc3_iir_in is output from the decimator 1 = adc3_iir_in is the DAC FIFO output
5	ADC_TEST_CTRL3 [5]	0	R/W	Enables loopback from the DAC FIFO to the ADC2 IIR input. Because the adc2 decimator out write signal is read for the DAC FIFO in this test mode, adc2 must be enabled to test any of the ADC IIR and other test signals are used to bypass the decimator out with interpolator in for the IIR: 0 = adc2_iir_in is output from the decimator 1 = adc2_iir_in is the DAC FIFO output
4	ADC_TEST_CTRL3 [4]	0	R/W	Enables loopback from the DAC FIFO to the ADC1 IIR input. Because the adc1 decimator out write signal is read for the DAC FIFO in this test mode, adc1 must be enabled to test any of the ADC IIR and other test signals are used to bypass the decimator out with interpolator in for the IIR: 0 = adc1_iir_in is output from the decimator 1 = adc1_iir_in is the DAC FIFO output
3	ADC_TEST_CTRL3 [3]	0	R/W	Enables loopback from the DAC interpolator engine to the ADC4 decimation engine at $F_s \times 8$ times. For this mode, the sample rate of both the DAC and ADC need to be set the same: 1 = Enables loopback 0 = Disables loopback
2	ADC_TEST_CTRL3 [2]	0	R/W	Enables loopback from the DAC interpolator engine to the ADC3 decimation engine at $F_s \times 8$ times. For this mode, the sample rate of both the DAC and ADC need to be set the same: 1 = Enables loopback 0 = Disables loopback

Table 156: ADC_TEST_CTRL3—0x19 (Continued)

Bits	Name	Default	R/W	Description
1	ADC_TEST_CTRL3 [1]	0	R/W	Enables loopback from the DAC interpolator engine to the ADC2 decimation engine at $F_s \times 8$ times. For this mode, the sample rate of both the DAC and ADC need to be set the same: • 1 = Enables loopback • 0 = Disables loopback
0	ADC_TEST_CTRL3 [0]	0	R/W	Enables loopback from the DAC interpolator engine to the ADC1 decimation engine at $F_s \times 8$ times. For this mode, the sample rate of both the DAC and ADC need to be set the same: • 1 = Enables loopback • 0 = Disables loopback

ADC_TEST_CTRL4—0x1A**Table 157: ADC_TEST_CTRL4—0x1A**

Bits	Name	Default	R/W	Description
7:6	ADC_TEST_CTRL4 [7:6]	0	R/W	Controls when the PGA comparison needs to be done for ADC4. The gain compare result is used for the gain ramping section in the PGA: 00 = Gain comparison at F_s 01 = Gain comparison at $F_s/2$ 10 = Gain comparison at $F_s/4$ 11 = Gain checking at $4 \cdot F_s$
5:4	ADC_TEST_CTRL4 [5:4]	0	R/W	Controls when the PGA comparison needs to be done for ADC3. The gain compare result is used for the gain ramping section in the PGA: 00 = Gain comparison at F_s 01 = Gain comparison at $F_s/2$ 10 = Gain comparison at $F_s/4$ 11 = Gain checking at $4 \cdot F_s$
3:2	ADC_TEST_CTRL4 [3:2]	0	R/W	Controls when the PGA comparison needs to be done for ADC2. The gain compare result is used for the gain ramping section in the PGA: 00 = Gain comparison at F_s 01 = Gain comparison at $F_s/2$ 10 = Gain comparison at $F_s/4$ 11 = Gain checking at $4 \cdot F_s$
1:0	ADC_TEST_CTRL4 [1:0]	0	R/W	Controls when the PGA comparison needs to be done for ADC1. The gain compare result is used for the gain ramping section in the PGA: 00 = Gain comparison at F_s 01 = Gain comparison at $F_s/2$ 10 = Gain comparison at $F_s/4$ 11 = Gain checking at $4 \cdot F_s$

MIXER0_PGA—0x1B**Table 158: MIXER0_PGA—0x1B**

Bits	Name	Default	R/W	Description
7	MIXER0_PGA_1[3]	0	R/W	Mixer mute for ADC channel 2: • 1 = Mutes the mixer input from ADC channel 2 • 0 = No mute
6:4	MIXER0_PGA_1[2:0]	1	R/W	Mixer PGA for ADC channel 2. The gain on the input data from ADC2 channel: • 000 = 2dB • 001 = 0dB • 010 = -2.5dB • 011 = -6dB • 100 = -12dB • 101 = -18dB • 110 = -24dB • 111 = -30dB
3	MIXER0_PGA_0[3]	0	R/W	Mixer mute for ADC channel 1: • 1 = Mutes the mixer input from ADC channel 1 • 0 = No mute
2:0	MIXER0_PGA_0[2:0]	1	R/W	Mixer PGA for ADC channel 1. The gain on the input data from ADC1 channel: • 000 = 2dB • 001 = 0dB • 010 = -2.5dB • 011 = -6dB • 100 = -12dB • 101 = -18dB • 110 = -24dB • 111 = -30dB

MIXER1_PGA—0x1C**Table 159: MIXER1_PGA—0x1C**

Bits	Name	Default	R/W	Description
7	MIXER1_PGA_1[3]	0	R/W	Mixer mute for ADC channel 4: 1 = Mutes the mixer input from ADC channel 4 0 = No mute
6:4	MIXER1_PGA_1[2:0]	0	R/W	Mixer PGA for ADC channel 4. The gain on the input data from the ADC4 channel: 000 = 2dB 001 = 0dB 010 = -2.5dB 011 = -6dB 100 = -12dB 101 = -18dB 110 = -24dB 111 = -30dB
3	MIXER1_PGA_0[3]	0	R/W	Mixer mute for ADC channel 3: 1 = Mutes the mixer input from ADC channel 3 0 = No mute
2:0	MIXER1_PGA_0[2:0]	0	R/W	Mixer PGA for ADC channel 3. The gain on the input data from the ADC3 channel: 000 = 2dB 001 = 0dB 010 = -2.5dB 011 = -6dB 100 = -12dB 101 = -18dB 110 = -24dB 111 = -30dB

DSP_CLK_CTRL—0x1D**Table 160: DSP_CLK_CTRL—0x1D**

Bits	Name	Default	R/W	Description
7:4	Reserved	0	-	Reserved.
3	DSP_CLK_CTRL [3]	0	R/W	Clock gate enable for the IIR biquad on ADC4: 0 = Disables the clock to the IIR biquad 1 = Enables the clock to the IIR biquad
2	DSP_CLK_CTRL [2]	0	R/W	Clock gate enable for the IIR biquad on ADC3: 0 = Disables the clock to the IIR biquad 1 = Enables the clock to the IIR biquad
1	DSP_CLK_CTRL [1]	0	R/W	Clock gate enable for the IIR biquad on ADC2: 0 = Disables the clock to the IIR biquad 1 = Enables the clock to the IIR biquad
0	DSP_CLK_CTRL [0]	0	R/W	Clock gate enable for the IIR biquad on ADC1: 0 = Disables the clock to the IIR biquad 1 = Enables the clock to the IIR biquad

MIC_OFFSET_CLK_CTRL—0x1E**Table 161: MIC_OFFSET_CLK_CTRL—0x1E**

Bits	Name	Default	R/W	Description
7:5	Reserved	0	-	Reserved.
4	MIC_OFFSET_CLK_DIV [4]	0	R/W	Enable for the microphone offset calibration clock divisor change. The divisor value on MIC_OFFSET_CLK_DIV[3:0] is latched when there is a 0-to-1 transition on this bit.
3:0	MIC_OFFSET_CLK_DIV [3:0]	3	R/W	Divider control for the microphone offset calibration clock. offset_clock = source_clock / (MIC_OFFSET_CLK_DIV[3:0] + 1) The source clock can be SYS CLOCK/4. The default is 0x3 to achieve a 768kHz calibration clock.

ADC1_PGA_LSB—0x20**Table 162: ADC1_PGA_LSB—0x20**

Bits	Name	Default	R/W	Description
7:0	ADC1_PGA_LSB [7:0]	0x58	R/W	Sets the digital PGA for the ADC1 channel. Program this LSB register first, followed by the MSB register for the gain value to be effective. See Table 163 for details.

ADC1_PGA_MSB—0x21**Table 163: ADC1_PGA_MSB—0x21**

Bits	Name	Default	R/W	Description
7:4	Reserved	0	-	Reserved.
3:2	ADC1_PGA_MSB [3:2]	0	R/W	Controls the ramping steps for the ADC1 digital PGA: 00 = Steps at ± 0.125dB 01 = Steps at ± 0.25dB 10 = Steps at ± 0.5dB 11 = Steps at ± 1dB
1:0	ADC1_PGA_MSB [9:8]	0x2	R/W	Sets the digital PGA for the ADC1 channel. Program the LSB register first, followed by this MSB register for the gain value to be effective. The gain is calculated by: $[(-75) + ((0.125) * (\text{decimal value of ADC1_PGA_MSB:LSB}))]$ Example: - To set 0dB gain with 0.125dB steps, write: 0x58 to ADC1_PGA_LSB[7:0] 0x02 to ADC1_PGA_MSB[9:8] - To set -20dB gain with 0.125dB steps, write: 0xB8 to ADC1_PGA_LSB[7:0] 0x01 to ADC1_PGA_MSB[9:8]

ADC2_PGA_LSB—0x22**Table 164: ADC2_PGA_LSB—0x22**

Bits	Name	Default	R/W	Description
7:0	ADC2_PGA_LSB [7:0]	0x58	R/W	Sets the digital PGA for the ADC2 channel. Program this LSB register first, followed by the MSB register for the gain value to be effective. See Table 165 for details.

ADC2_PGA_MSB—0x23**Table 165: ADC2_PGA_MSB—0x23**

Bits	Name	Default	R/W	Description
7:4	Reserved	0	-	Reserved.
3:2	ADC2_PGA_MSB [3:2]	0	R/W	Controls the ramping steps for the ADC2 digital PGA: • 00 = Steps at ±0.125dB • 01 = Steps at ±0.25dB • 10 = Steps at ±0.5dB • 11 = Steps at ±1dB
1:0	ADC2_PGA_MSB [9:8]	0x2	R/W	Sets the digital PGA for the ADC2 channel. Program the LSB register first, followed by this MSB register for the gain value to be effective. The gain is calculated by: $[(-75) + ((0.125) * (\text{decimal value of ADC2_PGA_MSB:LSB}))]$ Example: – To set 0dB gain with 0.125dB steps, write: • 0x58 to ADC2_PGA_LSB[7:0] • 0x02 to ADC2_PGA_MSB[9:8] – To set –20dB gain with 0.125dB steps, write: • 0xB8 to ADC2_PGA_LSB[7:0] • 0x01 to ADC2_PGA_MSB[9:8]

ADC3_PGA_LSB—0x24**Table 166: ADC3_PGA_LSB—0x24**

Bits	Name	Default	R/W	Description
7:0	ADC3_PGA_LSB [7:0]	0x58	R/W	Sets the digital PGA for the ADC3 channel. Program this LSB register first, followed by the MSB register for the gain value to be effective. See Table 167 for details.

ADC3_PGA_MSB—0x25**Table 167:** ADC3_PGA_MSB—0x25

Bits	Name	Default	R/W	Description
7:4	Reserved	0	-	Reserved.
3:2	ADC3_PGA_MSB [3:2]	0	R/W	Controls the ramping steps for the ADC3 digital PGA: • 00 = Steps at ±0.125dB • 01 = Steps at ±0.25dB • 10 = Steps at ±0.5dB • 11 = Steps at ±1dB
1:0	ADC3_PGA_MSB [9:8]	0x2	R/W	Sets the digital PGA for the ADC3 channel. Program the LSB register first, followed by this MSB register for the gain value to be effective. The gain is calculated by: $[(-75) + ((0.125) * (\text{decimal value of ADC3_PGA_MSB:LSB}))]$ Example: – To set 0dB gain with 0.125dB steps, write: • 0x58 to ADC3_PGA_LSB[7:0] • 0x02 to ADC3_PGA_MSB[9:8] – To set –20dB gain with 0.125dB steps, write: • 0xB8 to ADC3_PGA_LSB[7:0] • 0x01 to ADC3_PGA_MSB[9:8]

ADC4_PGA_LSB—0x26**Table 168:** ADC4_PGA_LSB—0x26

Bits	Name	Default	R/W	Description
7:0	ADC4_PGA_LSB [7:0]	0x58	R/W	Sets the digital PGA for the ADC4 channel. Program this LSB register first, followed by the MSB register for the gain value to be effective. See Table 169 for details.

ADC4_PGA_MSB—0x27**Table 169:** ADC4_PGA_MSB—0x27

Bits	Name	Default	R/W	Description
7:4	Reserved	0	-	Reserved.
3:2	ADC4_PGA_MSB [3:2]	0	R/W	Controls the ramping steps for the ADC4 digital PGA: • 00 = Steps at $\pm 0.125\text{dB}$ • 01 = Steps at $\pm 0.25\text{dB}$ • 10 = Steps at $\pm 0.5\text{dB}$ • 11 = Steps at $\pm 1\text{dB}$
1:0	ADC4_PGA_MSB [9:8]	0x2	R/W	Sets the digital PGA for the ADC4 channel. Program the LSB register first, followed by this MSB register for the gain value to be effective. The gain is calculated by: $[(-75) + ((0.125) * (\text{decimal value of ADC4_PGA_MSB:LSB}))]$ Example: – To set 0dB gain with 0.125dB steps, write: • 0x58 to ADC4_PGA_LSB[7:0] • 0x02 to ADC4_PGA_MSB[9:8] – To set –20dB gain with 0.125dB steps, write: • 0xB8 to ADC4_PGA_LSB[7:0] • 0x01 to ADC4_PGA_MSB[9:8]

Digital-to-Analog Converter (DAC)/Pulse-Width Modulation (PWM) Registers

DAC_EN_GAIN—0x28

Table 170: DAC_EN_GAIN—0x28

Bits	Name	Default	R/W	Description
7:1	DAC GAIN	0x4A	R/W	Programmable gain in digital: • 0x4F = 5dB • 0x4E = 4dB • 0x4D = 3dB • 0x4C = 2dB • ... • 0x3 = -71dB • 0x2 = -72dB • 0x1 = -73dB • 0x0 = -74dB
0	DAC/PWM ENABLE	0	R/W	• 0 = Disables the PWM chain • 1 = Enables the PWM chain

DAC_RATE_PWM_ATTN—0x29

Table 171: DAC_RATE_PWM_ATTN—0x29

Bits	Name	Default	R/W	Description
7	MUTE	0	R/W	Mutes the DAC out.
6:4	SAMPLE_RATE	0x4	R/W	• X0 = 8kHz • X1 = 16kHz • X2 = 24kHz • X3 = 32kHz • X4 = 48kHz • X5 = 96kHz • X6, X7 = Reserved
3	RAMP_STEP	0	R/W	Ramp step size: • 0 = 8 • 1 = 16
2	SIGNAL RAMP ENABLE	0	R/W	• 0 = Disables the signal ramp • 1 = Enables the signal ramp
1:0	ATT_SEL	0	R/W	• 00 = 0.4dB attenuation • 01 = 0.3dB attenuation • 10 = 0.2dB attenuation • 11 = No attenuation

HP_FILT_PWN_EN—0x2A**Table 172: HP_FILT_PWN_EN—0x2A**

Bits	Name	Default	R/W	Description
7	PWM_ANA_EN	0	R/W	Enables the PWM analog driver.
6:1	HP_BAND_SEL	0	R/W	Band selection for the high-pass. When hp_band_sel is: 0 = High-pass internally gets 'd4 - Programmed other than 0 = Whatever is programmed decides the band HPF frequency selection N * 30: 0x00 = 120Hz 0x01 = 30Hz 0x02 = 60Hz ... 0x3E = 1860Hz 0x3F = 1890Hz
0	HP_FILTER_EN	0	R/W	HPF enable for the DAC: 0 = Disable 1 = Enable

DAC_CEN_CTRL—0x2B**Table 173: DAC_CEN_CTRL—0x2B**

Bits	Name	Default	R/W	Description
7:2	Reserved	-	-	Reserved.
1:0	DAC_CEN_CTRL	0	R/W	Chip enable control for the DAC memories: 00 = CEN is driven low only when accessing 01 = CEN is driven low when the DAC is enabled 10/11 = Driven low all the time

Built-In Self-Test (BIST) Control and Status Registers

EQ_COEFF_BIST_STATUS—0x2C

Table 174: EQ_COEFF_BIST_STATUS—0x2C

Bits	Name	Default	R/W	Description
7	Reserved	-	-	Reserved.
6	IIR_MEM_CEN_CTRL	0	R/W	CEN control. The CEN is active low only when memory is being accessed, otherwise it is high. Set this bit to 1 to override and keep CEN low when the block is active.
5:0	Reserved	-	-	Reserved.

BIST_EN_MEM_STATUS—0x2D

Table 175: BIST_EN_MEM_STATUS—0x2D

Bits	Name	Default	R/W	Description
7	BIST_IIR_MEM4_STATUS	0	R	IIR mem4 status: 0 = Built-In Self-Test (BIST) test pass 1 = BIST test fail
6	BIST_IIR_MEM3_STATUS	0	R	IIR mem3 status: 0 = BIST test pass 1 = BIST test fail
5	BIST_IIR_MEM2_STATUS	0	R	IIR mem2 status: 0 = BIST test pass 1 = BIST test fail
4	BIST_IIR_MEM1_STATUS	0	R	IIR mem1 status: 0 = BIST test pass 1 = BIST test fail
3	DAC_MEM2_STATUS	0	R	DAC mem2 status: 0 = BIST test pass 1 = BIST test fail
2	DAC_MEM1_STATUS	0	R	DAC mem1 status: 0 = BIST test pass 1 = BIST test fail
1	BIST DONE	0	R	BIST complete signal.
0	BIST_TEST_START	0	R/W	1 = Start the BIST test 0 = Memory functional mode

ADC_MEM_STATUS—0x2E**Table 176: ADC_MEM_STATUS—0x2E**

Bits	Name	Default	R/W	Description
7	ADC_MEM8_STATS	0	R	ADC mem8 BIST status: 0 = BIST test pass 1 = BIST test fail
6	ADC_MEM7_STATS	0	R	ADC mem7 BIST status: 0 = BIST test pass 1 = BIST test fail
5	ADC_MEM6_STATS	0	R	ADC mem6 BIST status: 0 = BIST test pass 1 = BIST test fail
4	ADC_MEM5_STATS	0	R	ADC mem5 BIST status: 0 = BIST test pass 1 = BIST test fail
3	ADC_MEM4_STATS	0	R	ADC mem4 BIST status: 0 = BIST test pass 1 = BIST test fail
2	ADC_MEM3_STATS	0	R	ADC mem3 BIST status: 0 = BIST test pass 1 = BIST test fail
1	ADC_MEM2_STATS	0	R	ADC mem2 BIST status: 0 = BIST test pass 1 = BIST test fail
0	ADC_MEM1_STATS	0	R	ADC mem1 BIST status: 0 = BIST test pass 1 = BIST test fail

DAC_POST_RAMP—0x2F**Table 177: DAC_POST_RAMP—0x2F**

Bits	Name	Default	R/W	Description
7:0	DAC POST RAMP Count	0x14	R/W	DAC post ramp count.

I²S/DSP Registers

I2SDSP_CTRL_1—0x30

Table 178: I2SDSP_CTRL_1—0x30

Bits	Name	Default	R/W	Description
7	FIVE_MODE	0	R/W	Sets the audio interface in five-wire mode: 0 = Seven mode 1 = Five-wire mode In five-wire mode, the DAC bit clock and DAC LRCK are used for the ADC bit clock and ADC LRCK. The pins on the ADC bit clock and ADC LRCK are unused.
6	FIVE_CLK_LRCK	0	R/W	Selects whether the ADC or DAC control signals (CLK, LRCK) are used in five-wire mode: 0 = DAC CLK and LRCK are used 1 = ADC CLK and LRCK are used Note: Should be used only in five-wire mode.
5	Reserved	-	-	Reserved.
4:3	TX_SA_SIZE	0	R/W	Tx sample size control: 00 = 8-bit data 01 = 16-bit data 10 = 24-bit data 11 = Reserved
2:1	RX_SA_SIZE	0	R/W	Rx sample size control: 00 = 8-bit data 01 = 16-bit data 10 = 24-bit data 11 = Reserved
0	I2S_DSP_SEL	0	R/W	Mode select: 0 = Normal mode enable in I²S, left-justified, and right-justified 1 = Normal mode enable in DSP and TDM mode enable in I²S, left-justified, right-justified, and DSP

I2SDSP_CTRL_2—0x31**Table 179:** I2SDSP_CTRL_2—0x31

Bits	Name	Default	R/W	Description
7	LOOPBACK_ENABLE	0	R/W	Loopback enable bit that is used as a test mode to loopback data from the DAC to ADC, or the ADC to DAC (see the LOOPBACK_TYPE field): 0 = Disables the loopback 1 = Enables the loopback Note: Loopback feature testing also needs the proper setting of the LOOPBACK_MUX_SEL and LOOPBACK_TYPE fields.
6:5	LOOPBACK_MUX_SEL	0	R/W	Loopback ADC mux select: 00 = Selects the ADC1 channel for loopback 01 = Selects the ADC2 channel for loopback 10 = Selects the ADC3 channel for loopback 11 = Selects the ADC4 channel for loopback
4:0	TX_FRM_LEN	0	R/W	When in master mode, the Tx frame length in terms of bit clock cycles—it is $(N+1) * 8$: 00000 = 8 clocks per frame 00001 = 16 clocks per frame 00010 = 24 clocks per frame 00011 = 32 clocks per frame 11111 = 256 clocks per frame

I2SDSP_CTRL_3—0x32**Table 180:** I2SDSP_CTRL_3—0x32

Bits	Name	Default	R/W	Description
7	LOOPBACK_TYPE	0	R/W	Selects the type of loopback: 0 = DAC to ADC loopback 1 = ADC to DAC loopback
6:5	Reserved	-	-	Reserved.
4:0	RX_FRM_LEN	0	R/W	When in master mode, the Rx frame length in terms of bit clock cycles—it is $(N+1) * 8$: 00000 = 8 clocks per frame 00001 = 16 clocks per frame 00010 = 24 clocks per frame 00011 = 32 clocks per frame 11111 = 256 clocks per frame

I2SDSP_MST_CTRL_1—0x33**Table 181:** *I2SDSP_MST_CTRL_1—0x33*

Bits	Name	Default	R/W	Description
7	DSP_TDM_TX_CLK_INV	0	R/W	Inverts the Tx clock in the master mode of the DSP mode that runs on the negative edge of the clock and in I2S_TDM mode: 0 = Do not invert the Tx clock (default) 1 = Invert the Tx clock Note: This bit should only be used in I2S_TDM and DSP modes that run on the negative edge of the Tx clock.
6:0	TX_WS_WID	0	R/W	When in master mode, the Tx WS (sync/LRCK) high phase width in terms of bit clock cycles: 0000000 = 1 cycle 0000001 = 2 cycle 1111111 = 128 cycles

I2SDSP_MST_CTRL_2—0x34**Table 182:** *I2SDSP_MST_CTRL_2—0x34*

Bits	Name	Default	R/W	Description
7	DSP_TDM_RX_CLK_INV	0	R/W	Inverts the Rx clock in the master mode of the DSP mode that runs on the negative edge of the clock and in I2S_TDM mode: 0 = Do not invert the Rx clock (default) 1 = Invert the Rx clock Note: This bit should only be used in I2S_TDM and DSP modes that run on the negative edge of the Rx clock.
6:0	RX_WS_WID	0	R/W	When in master mode, the Rx WS (sync/LRCK) high phase width in terms of bit clock cycles: 0000000 = 1 cycle 0000001 = 2 cycle 1111111 = 128 cycles

I2S_TX_CTRL_1—0x35**Table 183: I2S_TX_CTRL_1—0x35**

Bits	Name	Default	R/W	Description
7	I2S1_TX_EN	0	R/W	Enables the I ² S-1 Tx when in I ² S, left-justified and right-justified normal operation mode.
6	I2S1_TX_MUTE	0	R/W	Mutes the I ² S-1 Tx (all zeros are sent).
5	I2S2_TX_EN	0	R/W	Enables I ² S-2 Tx when in I ² S, left-justified, and right-justified normal operation mode.
4	I2S2_TX_MUTE	0	R/W	Mutes the I ² S-2 Tx (all zeros are sent).
3	I2S_TX_WSPOL	0	R/W	A test mode control signal to invert the Tx (ADC) WS (LRCK) polarity: 0 = Polarity as per mode selected 1 = Invert polarity In: - I²S mode, the left channel data is on low WS - Left-justified mode and right-justified mode, the left channel data is on high WS If I2S_TX_WSPOL is set HIGH in: - Default I²S mode, the left channel data is on high WS - Left-justified and right-justified mode, the left channel data is on low WS
2:1	I2S_TX_MODE_SEL	0	R/W	Selects the mode for the Tx normal mode: 00 = I²S 01 = Left-justified 10 = Right-justified 11 = Reserved
0	Reserved	-	-	Reserved.

I2S_TX_CTRL_2—0x36**Table 184: I2S_TX_CTRL_2—0x36**

Bits	Name	Default	R/W	Description
7	Reserved	-	-	Reserved.
6:0	I2S_TX_BCNT_DLY	0	R/W	Only used in right-justified normal mode. If right-justified, this value indicates (N+1) delays in bit clock cycles for the first valid data transmitted: 7'h00 = 1 bit clock delay 7'h01 = 2 bit clock delay - Etc.

I2S_RX_CTRL_1—0x37**Table 185: I2S_RX_CTRL_1—0x37**

Bits	Name	Default	R/W	Description
7	I2S_RX_EN	0	R/W	Enables the Rx when in I ² S, left-justified, and right-justified normal operation mode.
6	I2S_RX_MUTE	0	R/W	Mutes the Rx (all zeros are sent) when in I ² S, left-justified, and right-justified normal mode.
5	I2S_RX_ORDER	0	R/W	I ² S, left-justified, and right-justified Rx data order: 0 = Processor sends data on the left channel 1 = Processor sends data on the right channel
4	Reserved	-	-	Reserved.
3	I2S_RX_WSPOL	0	R/W	A test mode control signal to invert the Rx (DAC) WS (LRCK) polarity: 0 = Polarity as per mode selected 1 = Invert polarity In: - I²S mode, the left channel data is on low WS - Left-justified mode and right-justified mode, the left channel data is on high WS if I2S_RX_WSPOL is set HIGH in: - Default I²S mode, the left channel data is on high WS - Left-justified and right-justified mode, the left channel data is on low WS
2:1	I2S_RX_MODE_SEL	0	R/W	Selects the mode for the Tx in normal mode: 00 = I²S 01 = Left-justified 10 = Right-justified 11 = Reserved
0	Reserved	-	-	Reserved.

I2S_RX_CTRL_2—0x38**Table 186: I2S_RX_CTRL_2—0x38**

Bits	Name	Default	R/W	Description
7	Reserved	-	-	Reserved.
6:0	I2S_RX_BCNT_DLY	0	R/W	Only used in right-justified normal mode. If right-justified, this value indicates (N+1) delays in bit clock cycles for the first valid data transmitted: 7'h00 = 1 bit clock delay 7'h01 = 2 bit clock delay - Etc.

DSP_CTRL—0x39**Table 187: DSP_CTRL—0x39**

Bits	Name	Default	R/W	Description
7	DSP_TX_WSPOL	0	R/W	ADC LRCK inversion control: 0 = ADC LRCK is not inverted 1 = ADC LRCK is inverted This bit is only used in I ² S TDM modes.
6	DSP_RX_WSPOL	0	R/W	DAC LRCK inversion control: 0 = DAC LRCK is not inverted 1 = DAC LRCK is inverted This bit is only used in I ² S TDM modes.
5:4	Reserved	-	-	Reserved.
3	DSP_DSTART_DLY	0	R/W	DSP Tx and Rx data start delay control: 0 = Left-justified data is not delayed 1 = Left-justified data is delayed 1 bit Note: In DSP: - Slave short frame sync mode, DSP_DSTAT_DLY is set HIGH - Master short frame sync mode, set TX/RX_WS_WID to 7'h00 along with DSP_DSTAT_DLY This bit is also used in I ² S TDM mode.
2	DSP_DSHIFT_SEL	0	R/W	DSP Tx and Rx data shift select. Determines the data shift direction: 0 = MSB first 1 = LSB first
1	DSP_TX_OUT_LINE_SEL	0	R/W	0 = DSP sends ADC1, ADC2 data on sdata1 (tx_data_1) and ADC3, and ADC4 data on sdata2 (tx_data_2) 1 = DSP sends all four channels of ADC data on sdata1(tx_data_1)
0	DSP_TX_TRI_N	0	R/W	Enables the DSP Tx output enable only for the slots that are actively supposed to drive: 0 = Tristate 1 = Do not tristate This bit is used in all the TDM modes.

DSP_TX_CTRL_1—0x3A**Table 188: DSP_TX_CTRL_1—0x3A**

Bits	Name	Default	R/W	Description
7:5	Reserved	-	-	Reserved.
4:0	DSP_TX_SLOT_1	0	R/W	First slot number for Tx channel 1. Each slot is 8 bits. All the enabled Tx channels should be configured with unique slot numbers. Note: If the Tx sample size is 16 or 24, it uses two or three consecutive slots respectively.

DSP_TX_CTRL_2—0x3B**Table 189: DSP_TX_CTRL_2—0x3B**

Bits	Name	Default	R/W	Description
7:5	Reserved	-	-	Reserved.
4:0	DSP_TX_SLOT_2	0	R/W	First slot number for Tx channel 2. Each slot is 8 bits. All the enabled Tx channels should be configured with unique slot numbers. Note: If the Tx sample size is 16 or 24, it uses two or three consecutive slots respectively.

DSP_TX_CTRL_3—0x3C**Table 190: DSP_TX_CTRL_3—0x3C**

Bits	Name	Default	R/W	Description
7:5	Reserved	-	-	Reserved.
4:0	DSP_TX_SLOT_3	0	R/W	First slot number for Tx channel 3. Each slot is 8 bits. All the enabled Tx channels should be configured with unique slot numbers. Note: If the Tx sample size is 16 or 24, it uses two or three consecutive slots respectively.

DSP_TX_CTRL_4—0x3D**Table 191: DSP_TX_CTRL_4—0x3D**

Bits	Name	Default	R/W	Description
7:5	Reserved	-	-	Reserved.
4:0	DSP_TX_SLOT_4	0	R/W	First slot number for Tx channel 4. Each slot is 8 bits. All the enabled Tx channels should be configured with unique slot numbers. Note: If the Tx sample size is 16 or 24, it uses two or three consecutive slots respectively.

DSP_TX_CTRL_5—0x3E**Table 192: DSP_TX_CTRL_5—0x3E**

Bits	Name	Default	R/W	Description
7	Reserved	-	-	Reserved.
6:5	DSP_LAST_ADC_CH	0		Channel number that represents the last channel in a frame: 0x0 = Channel 1 is the last channel in a frame 0x1 = Channel 2 is the last channel in a frame 0x2 = Channel 3 is the last channel in a frame 0x3 = Channel 4 is the last channel in a frame
4	DSP_LAST_ADC_CH_EN	0		Enables to use the last channel programmed in the DSP_LAST_ADC_CH field. 1 = Enable 0 = Disable (use the default) Note: This bit should be enabled only if the Tx channels are not in ascending order (i.e., tx_slot1 < tx_slot2 < tx_slot3 < tx_slot4).
3	DSP_TX_EN_4	0	R/W	Enables the Tx on channel 4 if the data interface is set to DSP normal operation mode or any TDM mode.
2	DSP_TX_EN_3	0	R/W	Enables the Tx on channel 3 if the data interface is set to DSP normal operation mode or any TDM mode.
1	DSP_TX_EN_2	0	R/W	Enables the Tx on channel 2 if the data interface is set to DSP normal operation mode or any TDM mode.
0	DSP_TX_EN_1	0	R/W	Enables the Tx on channel 1 if the data interface is set to DSP normal operation mode or any TDM mode.

DSP_RX_CTRL_1—0x3F**Table 193: DSP_RX_CTRL_1—0x3F**

Bits	Name	Default	R/W	Description
7	DSP_RX_EN	0	R/W	Enables the Rx on channel 1 in DSP normal operation mode or any TDM mode.
6:5	Reserved	-	-	Reserved.
4:0	DSP_RX_SLOT_1	0	R/W	First slot number for Rx channel 1. Each slot is 8 bits. Note: If the Rx sample size is 16 or 24, it uses two or three consecutive slots respectively.

FIFO_CTRL—0x40

The FIFO_CTRL register is a control register used to flush the FIFOs. This register is applicable for all modes.

Table 194: FIFO_CTRL—0x40

Bits	Name	Default	R/W	Description
7:5	Reserved	-	-	Reserved.
4	ADC4_FIFO_FLUSH	0	R/W	Flushes the ADC4 FIFO: 1 = Flushes the FIFO 0 = Does not flush the FIFO (for normal operation)
3	ADC3_FIFO_FLUSH	0	R/W	Flushes the ADC3 FIFO: 1 = Flushes the FIFO 0 = Does not flush the FIFO (for normal operation)
2	ADC2_FIFO_FLUSH	0	R/W	Flushes the ADC2 FIFO: 1 = Flushes the FIFO 0 = Does not flush the FIFO (for normal operation)
1	ADC1_FIFO_FLUSH	0	R/W	Flushes the ADC1 FIFO: 1 = Flushes the FIFO 0 = Does not flush the FIFO (for normal operation)
0	DAC_FIFO_FLUSH	0	R/W	Flushes DAC FIFO: 1 = Flushes the FIFO 0 = Does not flush the FIFO (for normal operation)

Direct Current (DC) Protection Registers

DC_PROT_0—0x55

Table 195: DC_PROT_0—0x55

Bits	Name	Default	R/W	Description
7	DC_DET_STATUS	0	R	DC detect status bit. When this bit is set, Pwm_ana_en is driven 0 until it is cleared by the DC_DET_CLEAR bit.
6	DC_DET_CLEAR	0	R/W	Used to clear the DC_DET_STATUS bit.
5:4	DC_LP_BAND_SEL	0	R/W	LPF band selection for DC detection: 00 = 1.3s 01 = 1.3s 10 = 680ms 11 = 450ms
3:2	THRESHOLD_SEL	0	R/W	Threshold for a shutdown decision for DC detection on speakers: 00 = 5% 01 = 10% 10 = 15% 11 = 20%
1	FILTER_METHOD_EN	0	R/W	DC detection through the filter or counter: 0 = Counter method to detect a DC 1 = Filter method to detect a DC
0	DC_PROT_EN	0	R/W	DC protection enable for the DAC PWM.

DC_PROT_1—0x56

Table 196: DC_PROT_1—0x56

Bits	Name	Default	R/W	Description
7:1	Reserved	-	-	Reserved.
0	PWM_AN_EN_CTRL	0	R/W	PWM ANA enable control: 0 = pwm_ana_en goes as-is to the analog driver 1 = pwm_ana_en DC detection control—pwm_ana_en is disabled when a DC is detected

PLL Control Registers

PLL_CTRL_1—0x60

Table 197: PLL_CTRL_1—0x60

Bits	Name	Default	R/W	Description
7	PLL1_DIVOUT_EN2P5	0	R/W	Enables the additional divide-by-2.5 on the PLL1 output.
6:4	PLL1_DIVOUT	0	R/W	Output divider selection for PLL1—divide ratio = PLL1_DIVOUT+1.
3	PLL1_N[8]	0	R/W	MSB of the 9-bit integer part of the PLL1 feedback divider.
2	PLL1_BYPASS	0	R/W	Bypasses PLL1: 0 = Clock output is from the PLL1 output 1 = Clock output is from the CODEC digital
1	PLL1_RESETN	0	R/W	Active-low reset for PLL1 (1 = enable).
0	PLL1_EN	0	R/W	Enables PLL1 (1 = enable).

PLL_CTRL_2—0x61

Table 198: PLL_CTRL_2—0x61

Bits	Name	Default	R/W	Description
7:0	PLL1_N[7:0]	0	R/W	Eight LSBs of the 9-bit integer part of the PLL1 feedback divider—divide ratio = pll1_n + 1.

PLL_CTRL_3—0x62

Table 199: PLL_CTRL_3—0x62

Bits	Name	Default	R/W	Description
7:6	PLL1_BWCTRL	0	R/W	Loop filter tuning.
5:0	PLL1_DIVIN	0	R/W	Input divider selection for PLL1—divide ratio = pll1_divin + 1.

PLL_CTRL_4—0x63

Table 200: PLL_CTRL_4—0x63

Bits	Name	Default	R/W	Description
7:2	PLL1_COEFFSEL	0	R/W	Tune feedback coefficients in the PLL1 fractional modulator.
1	PLL1_DITHER_EN	0	R/W	Enables the dither for PLL1 (1 = enable).
0	PLL1_INTMODE	0	R/W	Enables the integer-only mode for PLL1 (1 = disable fractional modulator).

PLL_CTRL_5—0x64*Table 201: PLL_CTRL_5—0x64*

Bits	Name	Default	R/W	Description
7:0	PLL1_Frac[7:0]	0	R/W	Eight LSBs of the fractional part of the PLL1 feedback divider.

PLL_CTRL_6—0x65*Table 202: PLL_CTRL_6—0x65*

Bits	Name	Default	R/W	Description
7:0	PLL1_Frac[15:8]	0	R/W	Bits 15 to 8 of the fractional part of the PLL1 feedback divider.

PLL_CTRL_7—0x66*Table 203: PLL_CTRL_7—0x66*

Bits	Name	Default	R/W	Description
7	PLL2_CKDIVSEL	0	R/W	Bypasses the final output divider for the pll2_ckout: 0 = pll2_ckout is the output of the final output divider 1 = pll2_ckout is the input of the final output divider
6:4	PLL2_FINALDIV	0	R/W	pll2_ckout final output divider control—divide ratio = PLL2_FINALDIV+1.
3:0	PLL1_FRAC[19:16]	0	R/W	Four MSBs of the fractional part of the PLL1 feedback divider.

PLL_CTRL_8—0x67*Table 204: PLL_CTRL_8—0x67*

Bits	Name	Default	R/W	Description
7	PLL2_DIVOUT_EN2P5	0	R/W	Enables the additional divide-by-2.5 on the PLL2 output.
6:4	PLL2_DIVOUT	0	R/W	Output divider selection for PLL2—divide ratio = pll2_divout+1.
3	PLL2_N[8]	0	R/W	MSB of the 9-bit integer part of the PLL2 feedback divider.
2	PLL2_CKOUTSEL	0	R/W	Selects the pll2_ckout clock source: 0 = pll2_ckout is output of PLL1 1 = pll2_ckout is output of PLL2
1	PLL1_ENOUT	0	R/W	Enables the pll1_ckout output to the CODEC digital.
0	PLL2_EN	0	R/W	Enables PLL2 (1 = enable).

PLL_CTRL_9—0x68*Table 205: PLL_CTRL_9—0x68*

Bits	Name	Default	R/W	Description
7:0	PLL2_N[7:0]	0	R/W	Eight LSBs of the 9-bit integer part of the PLL2 feedback divider—divide ratio = PLL2_N + 1.

PLL_CTRL_10—0x69*Table 206: PLL_CTRL_10—0x69*

Bits	Name	Default	R/W	Description
7:6	PLL2_BWCTRL	0	R/W	Loop filter tuning.
5:0	PLL2_DIVIN	0	R/W	Input divider selection for PLL2—divide ratio = PLL2_DIVIN + 1.

PWM Analog Control Register

PWM_CTRL_1—0x70

Table 207: PWM_CTRL_1—0x70

Bits	Name	Default	R/W	Description
7:6	PWM_ATEST_CTRL	0	R/W	PWM analog test mux control: • 00 = No test • 01 = VBG to the atest_out pad • 10 = IREF to the atest_out pad • 11 = No test
5:3	PWM_VBG_CTRL	0	R/W	PWM driver bandgap reference trimming: • 000 = 1.239V • 001 = 1.265V • 010 = 1.292V • 011 = 1.319V • 100 = 1.131V • 101 = 1.158V • 110 = 1.184V • 111 = 1.211V
2:0	PWM_IREF_CTRL	0	R/W	PWM driver reference current trimming: • 000 = 5.04μA • 001 = 5.20μA • 010 = 5.39μA • 011 = 5.58μA • 100 = 4.45μA • 101 = 4.58μA • 110 = 4.72μA • 111 = 4.86μA

PWM_CTRL_2—0x71**Table 208: PWM_CTRL_2—0x71**

Bits	Name	Default	R/W	Description
7	Reserved	0	-	Reserved.
6	PWM_OC_ERR_CLEAR	0	R/W	Clears the long-term short-circuit oc_err sticky bit for the PWM driver. To reset the state, the bit must be written high to clear the sticky bit, and then written low to allow normal operation: 0 = Normal operation 1 = Resets/forces the oc_err sticky bit low
5	PWM_OC_ERR_RECOV_DIS	0	R/W	Disables the long-term short-circuit recovery mode in the PWM driver: 0 = Enables the recovery mode—if the oc_err sticky bit is set, the logic automatically resets the sticky bit after 5.5s 1 = Disables the recovery mode—if the oc_err sticky bit is set, the driver is disabled until the user resets the sticky bit or the driver is disabled/re-enabled
4:3	PWM_OC_WIN	0	R/W	PWM driver long-term, short-circuit measurement window (384kHz REF CLK): 00 = 1365ms 01 = 683ms 10 = 85ms 11 = 21ms
2:0	PWM_OC_THRESH	0	R/W	PWM driver long-term, short-circuit trip threshold (# of SC events): 000 = 131 001 = 65K 010 = 33K 011 = 16 100 = 8K 101 = 4K 110 = 2K 111 = 1K

PWM_CTRL_3—0x72**Table 209: PWM_CTRL_3—0x72**

Bits	Name	Default	R/W	Description
7:6	Reserved	0	-	Reserved.
5:4	PWM_DRIVER_SLEW	0	R/W	PWM pre-driver slew rate control (PWM output rise/fall time): • 00 = 0.25ns • 01 = 1ns • 10 = 2ns • 11 = 4ns
3	PWM_AUTODTC_DIS	0	R/W	PWM driver that disables the auto-DTC circuitry (i.e., can disable only if PWM_DRIVER_SLEW = 00): • 0 = Enables the auto-DTC circuitry • 1 = Disables the auto-DTC circuitry and uses a fixed dead-time period
2:0	PWM_DEADTIME	0	R/W	PWM pre-driver minimum dead-time programming: • 000 = 0.5ns • 001 = 1.8ns • 010 = 3.5ns • 011 = 4.1ns • 100 = 6ns • 001 = 6.6ns • 010 = 8.3ns • 011 = 8.9ns

PWM_CTRL_4—0x73**Table 210: PWM_CTRL_4—0x73**

Bits	Name	Default	R/W	Description
7	PWM_IMEAS_DIS	0	R/W	PWM driver disable short-circuit detection circuitry: 0 = Enables detection 1 = Disables and shuts off the detection
6	PWM_IMEAS_IGNORE	0	R/W	PWM forces the pre-drivers to ignore the short-circuit error signals while leaving the detection circuitry enabled (for test purposes): 0 = Uses detection circuitry to disable the pre-driver 1 = Pre-drivers ignore the detection circuitry
5:4	PWM_IMEAS_FILT	0	R/W	PWM driver short-circuit detection filter capacitor programmability: 00 = 50fF 01 = 100fF 10 = 200fF 11 = 400fF
3	PWM_IMEAS_DAC_LOWCURR	0	R/W	PWM driver forces the short-circuit threshold programming to low current settings (for ATE testing).
2:0	PWM_IMEAS_DAC	0	R/W	PWM driver short-circuit threshold programmability: - PWM_IMEAS_DAC_LOWCURR = 0 000 = 1.4A 001 = 1.6A 010 = 1.8A 011 = 2A 100 = 0.6A 101 = 0.8A 110 = 1A 111 = 1.2A - PWM_IMEAS_DAC_LOWCURR = 1 000 = 233mA 001 = 266mA 010 = 300mA 011 = 333mA 100 = 100mA 101 = 133mA 110 = 167mA 111 = 200mA

PWM_CTRL_5—0x74**Table 211: PWM_CTRL_5—0x74**

Bits	Name	Default	R/W	Description
7:4	PWM_TEMP_CTRL_RISE	0	R/W	PWM driver temperature sensor rising threshold: • 0000 = 130.7°C • 0001 = 140.2°C • 0010 = 152.9°C • 0011 = 171.1°C • 0100 = 103.6°C • 0101 = 111.3°C • 0110 = 116.7°C • 0111 = 123°C • 1000 = 45.4°C • 1001 = 55.9°C • 1010 = 70.1°C • 1011 = 91.2°C • 1100 = 16.6°C • 1101 = 24.7°C • 1110 = 30.4°C • 1111 = 37.1°C
3:0	PWM_TEMP_CTRL_FALL	0	R/W	PWM driver temperature sensor falling threshold: • 0000 = 111.3°C • 0001 = 103.6°C • 0010 = 123°C • 0011 = 116.7°C • 0100 = 140.2°C • 0101 = 130.7°C • 0110 = 171.1°C • 0111 = 152.9°C • 1000 = 24.7°C • 1001 = 16.6°C • 1010 = 37.1°C • 1011 = 30.4°C • 1100 = 55.9°C • 1101 = 45.4°C • 1110 = 91.2°C • 1111 = 70.1°C

PWM_CTRL_6—0x75**Table 212: PWM_CTRL_6—0x75**

Bits	Name	Default	R/W	Description
7	Reserved	0	-	Reserved.
6	PWM_FORCE_POR	0	R/W	PWM driver override POR output: 0 = Uses the POR circuitry output 1 = Forces the POR signal high
5	PWM_TEMP_DISABLE	0	R/W	PWM driver disable temperature sensor: 0 = Enables the temperature sensor 1 = Disables the temperature sensor and the output is forced low
4	PWM_CLK_DET_DISABLE	0	R/W	PWM driver disable clock detection circuitry: 0 = Enables the clock detector 1 = Disables the clock detector and the output is forced high
3	PWM_FORCE_HI_Z	0	R/W	PWM driver override for the high-Z control logic: 0 = Uses the high-Z logic output 1 = Forces the high-Z logic to output high
2	PWM_TEMP_FILT_BYPASS	0	R/W	PWM driver bypass temperature sensor blanking filter: 0 = Enables the filter (~80 us blanking) 1 = Bypasses the filter (0 blanking)
1:0	PWM_DIG_TESTMUX_SEL	0	R/W	PWM driver digital test mux control (routes signals to dig_testmux_out [3:0]): 00 = Long-term, short-circuit debug [en_win, win_count, oc_hit, oc_error_stick] 01 = Short-term, short-circuit debug [oc_pfet_p, oc_nfet_p, oc_pfet_m, oc_nfet_m] 10 = Temperature sensor logic debug [temp_err, temp_err_filt, tsense_q1, tsense_q0] 11 = Error debug [hi_z_ctrl, por_all, oc_error_stick, temp_err_filt]

ADC REF Control Register

REF_CTRL_1—0x78

Table 213: REF_CTRL_1—0x78

Bits	Name	Default	R/W	Description
7	Reserved	0	-	Reserved.
6	LDO33ANA_ENABLE	0	R/W	Enables the analog LDO: 0 = Shuts down the LDO—1.2mΩ resistance to the GND at the output pin 1 = Enables the LDO
5	VREF_ENABLE	0	R/W	Enables the VREF (needed for analog LDO and micbias): 0 = Disables the VREF 1 = Enables the VREF
4:0	VREF_SEL	0	R/W	Control VREF output and micbias voltage: - AVDD5 = 5V: - VREF = $1.5 + 0.1 \cdot \text{vref_sel}$ (maximum VREF is 4V → maximum vref_sel = 25 decimal) - AVDD5 = 3.3V: - VREF = $\text{AVDD5} \cdot (\text{vref_sel} + 15) / 36$ if headroom = 5% (0x79 [6] = 0) - VREF = $\text{AVDD5} \cdot (\text{vref_sel} + 15) / 38$ if headroom = 10% (0x79 [6] = 1) - VREF maximum is always $0.95 \cdot \text{AVDD5}$

REF_CTRL_2—0x79**Table 214:** REF_CTRL_2—0x79

Bits	Name	Default	R/W	Description
7	Reserved	0	-	Reserved.
6	LDO33ANA_2XHDRM	0	R/W	Controls the minimum headroom between the analog LDO input and output. At input supplies near the target output voltage, the output tracks lower to ensure good PSRR: 0 = LDO headroom is 5% 1 = LDO headroom is 10%
5	LDO33ANA_ILIM_DISABLE	0	R/W	Disables the output current limiting on the analog LDO: 0 = Enables the 50mA current limit 1 = Disables the current limit
4	VREF_FASTSTART_DISABLE	0	R/W	Disables the fast-start circuit on the VREF: 0 = Enables the fast-start 1 = Disables the fast-start
3:0	VREF_BG_TRIM [3:0]	0	R/W	Bandgap VREF trimming: 0 = 1.238V 1 = 1.232V 2 = 1.225V 3 = 1.219V 4 = 1.212V 5 = 1.205V 6 = 1.198V 7 = 1.192V 8 = 1.292V 9 = 1.286V 10 = 1.279V 11 = 1.272V 12 = 1.265V 13 = 1.258V 14 = 1.252V 15 = 1.245V

REF_CTRL_3—0x7A**Table 215:** REF_CTRL_3—0x7A

Bits	Name	Default	R/W	Description
7:1	Reserved	0	-	Reserved.
0	VREFP_ENABLE	0	R/W	Enables the VREFP (needed by all audio input channels).

REF_CTRL_4—0x7B**Table 216: REF_CTRL_4—0x7B**

Bits	Name	Default	R/W	Description
7	Reserved	0	-	Reserved.
6	VREFP_FASTSTART_DISABLE	0	R/W	Disables the fast-start circuit on VREFP.
5:4	VREFP_RESCTRL	0	R/W	Controls the output impedance of VREFP: 00 = 1mΩ 01 = 10mΩ 10 = Low impedance 11 = 100kΩ
3	VREFP_LPMODE	0	R/W	Enables the low-power mode for VREFP (used when the DSM_VREFP_LPMODE mode is set for all channels).
2:0	IGEN_TRIM	0	R/W	Tune bias current generator for all audio input channels: 000 = Nominal (5μA) 001 = -4.8% 010 = -9.1% 011 = -13% 100 = 25% 101 = 17.6% 110 = 11% 111 = 5.2%

ANA_CTRL_1—0x7C**Table 217: ANA_CTRL_1—0x7C**

Bits	Name	Default	R/W	Description
7:0	Reserved	0	-	Reserved.

ANA_CTRL_2—0x7D**Table 218: ANA_CTRL_2—0x7D**

Bits	Name	Default	R/W	Description
7:0	Reserved	0	-	Reserved.

Input/Output (I/O) Control Registers

MCLK_PAD_CTRL—0x80

Table 219: MCLK_PAD_CTRL—0x80

Bits	Name	Default	R/W	Description
7:4	Reserved	0	-	Reserved.
3:2	MCLK_PAD_CTRL[3:2]	0	R/W	Pad-programmable pull-up/pull-down control: 00 = No pull-up or pull-down 01 = Weak pull-down 10 = Weak pull-up value 1 → 10kΩ–35kΩ 11 = Weak pull-up value 2 → 130kΩ–315kΩ
1	Reserved	1	-	Reserved.
0	MCLK_PAD_CTRL[0]	0	R/W	Pad input enable: 1 = Pad is input-enabled 0 = Disables the pad input mode

I2S_PAD_CTRL—0x81

Table 220: I2S_PAD_CTRL—0x81

Bits	Name	Default	R/W	Description
7:5	Reserved	0	-	Reserved.
4:2	I2S_PAD_CTRL[4:2]	0x7	R/W	Pad-programmable drive control for rx_clk, rx_lrck, tx_clk, and tx_lrck: 000 = IOL/IOH = ±0.3mA 001 = IOL/IOH = ±1mA 010 = IOL/IOH = ±2.6mA 011 = IOL/IOH = ±3.3mA 100 = IOL/IOH = ±6.1mA 101 = IOL/IOH = ±6.8mA 110 = IOL/IOH = ±8.5mA 111 = IOL/IOH = ±9.2mA Note: For other I²S pad controls, see Table 179 on page 221 and Table 180 on page 221.
1:0	I2S_PAD_CTRL[1:0]	0	R/W	Pad-programmable pull-up/pull-down control for rx_clk, rx_lrck, tx_clk, tx_lrck: 00 = No pull-up or pull-down 01 = Weak pull-down → 130kΩ–450kΩ 10 = Weak pull-up value 1 → 10kΩ–35kΩ 11 = Weak pull-up value 2 → 130kΩ–315kΩ Note: For other I²S pad controls, see Table 179 on page 221 and Table 180 on page 221.

I2S_RX_PAD_CTRL—0x82**Table 221:** *I2S_RX_PAD_CTRL—0x82*

Bits	Name	Default	R/W	Description
7:6	Reserved	0	-	Reserved.
5	I2S_RX_PAD_CTRL[5]	0	R/W	Pad output enable (for rx_data): 0 = Pad is output-enabled 1 = Pad is not output-enabled
4	I2S_RX_PAD_CTRL[4]	0	R/W	Pad input enable (for rx_data): 1 = Pad is input-enabled 0 = Disables the pad input mode
3	I2S_RX_PAD_CTRL[3]	0	R/W	Pad output enable (for rx_lrck): 0 = Pad is output-enabled 1 = Pad is not output-enabled
2	I2S_RX_PAD_CTRL[2]	0	R/W	Pad input enable (for rx_lrck): 1 = Pad is input-enabled 0 = Disables the pad input mode
1	I2S_RX_PAD_CTRL[1]	0	R/W	Pad output enable (for rx_clk): 0 = Pad is output-enabled 1 = Pad is not output-enabled
0	I2S_RX_PAD_CTRL[0]	0	R/W	Pad input enable (for rx_clk): 1 = Pad is input-enabled 0 = Disables the pad input mode

I2S_TX_PAD_CTRL—0x83**Table 222: I2S_TX_PAD_CTRL—0x83**

Bits	Name	Default	R/W	Description
7	I2S_TX_PAD_CTRL[7]	0	R/W	Pad output enable (for TX_DATA_2): 0 = Pad is output-enabled 1 = Pad is not output-enabled
6	I2S_TX_PAD_CTRL[6]	0	R/W	Pad input enable (for TX_DATA_2): 1 = Pad is input-enabled 0 = Disables the pad input mode
5	I2S_TX_PAD_CTRL[5]	0	R/W	Pad output enable (for TX_DATA_1): 0 = Pad is output-enabled 1 = Pad is not output-enabled
4	I2S_TX_PAD_CTRL[4]	0	R/W	Pad input enable (for TX_DATA_1): 1 = Pad is input-enabled 0 = Disables the pad input mode
3	I2S_TX_PAD_CTRL[3]	0	R/W	Pad output enable (for tx_lrck): 0 = Pad is output-enabled 1 = Pad is not output-enabled
2	I2S_TX_PAD_CTRL[2]	0	R/W	Pad input enable (for tx_lrck): 1 = Pad is input-enabled 0 = Disables the pad input mode
1	I2S_TX_PAD_CTRL[1]	0	R/W	Pad output enable (for tx_clk): 0 = Pad is output-enabled 1 = Pad is not output-enabled
0	I2S_TX_PAD_CTRL[0]	0	R/W	Pad input enable (for tx_clk): 1 = Pad is input-enabled 0 = Disables the pad input mode

GPIO0_PAD_CTRL—0x84**Table 223:** GPIO0_PAD_CTRL—0x84

Bits	Name	Default	R/W	Description
7	Reserved	0	-	Reserved.
6:4	GPIO0_PAD_CTRL[6:4]	0	R/W	Pad-programmable drive control—the following values are for the 3.3V VDDO: • 000 = IOL/IOH = $\pm 0.3\text{mA}$ • 001 = IOL/IOH = $\pm 1\text{mA}$ • 010 = IOL/IOH = $\pm 2.6\text{mA}$ • 011 = IOL/IOH = $\pm 3.3\text{mA}$ • 100 = IOL/IOH = $\pm 6.1\text{mA}$ • 101 = IOL/IOH = $\pm 6.8\text{mA}$ • 110 = IOL/IOH = $\pm 8.5\text{mA}$ • 111 = IOL/IOH = $\pm 9.2\text{mA}$
3:2	GPIO0_PAD_CTRL[3:2]	0	R/W	Pad-programmable pull-up/pull-down control: • 00 = No pull-up or pull-down • 01 = Weak pull-down • 10 = Weak pull-up value 1 $\rightarrow 10\text{k}\Omega\text{--}35\text{k}\Omega$ • 11 = Weak pull-up value 2 $\rightarrow 130\text{k}\Omega\text{--}315\text{k}\Omega$
1	GPIO0_PAD_CTRL[1]	1	R/W	Pad output enable: • 0 = Pad is output-enabled • 1 = Pad is not output-enabled
0	GPIO0_PAD_CTRL[0]	0	R/W	Pad input enable: • 1 = Pad is input-enabled • 0 = Disables the pad input mode

GPIO1_PAD_CTRL—0x85**Table 224:** GPIO1_PAD_CTRL—0x85

Bits	Name	Default	R/W	Description
7	Reserved	0	-	Reserved.
6:4	GPIO1_PAD_CTRL[6:4]	0	R/W	Pad-programmable drive control—the following values are for the 3.3V VDDO: • 000 = IOL/IOH = $\pm 0.3\text{mA}$ • 001 = IOL/IOH = $\pm 1\text{mA}$ • 010 = IOL/IOH = $\pm 2.6\text{mA}$ • 011 = IOL/IOH = $\pm 3.3\text{mA}$ • 100 = IOL/IOH = $\pm 6.1\text{mA}$ • 101 = IOL/IOH = $\pm 6.8\text{mA}$ • 110 = IOL/IOH = $\pm 8.5\text{mA}$ • 111 = IOL/IOH = $\pm 9.2\text{mA}$
3:2	GPIO1_PAD_CTRL[3:2]	0	R/W	Pad-programmable pull-up/pull-down control: • 00 = No pull-up or pull-down • 01 = Weak pull-down • 10 = Weak pull-up value 1 $\rightarrow 10\text{k}\Omega\text{--}35\text{k}\Omega$ • 11 = Weak pull-up value 2 $\rightarrow 130\text{k}\Omega\text{--}315\text{k}\Omega$
1	GPIO1_PAD_CTRL[1]	1	R/W	Pad output enable: • 0 = Pad is output-enabled • 1 = Pad is not output-enabled
0	GPIO1_PAD_CTRL[0]	0	R/W	Pad input enable: • 1 = Pad is input-enabled • 0 = Disables the pad input mode

GPIO2_PAD_CTRL—0x86**Table 225: GPIO2_PAD_CTRL—0x86**

Bits	Name	Default	R/W	Description
7	Reserved	0	-	Reserved.
6:4	GPIO2_PAD_CTRL[6:4]	0	R/W	Pad-programmable drive control—the following values are for the 3.3V VDDO: • 000 = IOL/IOH = $\pm 0.3\text{mA}$ • 001 = IOL/IOH = $\pm 1\text{mA}$ • 010 = IOL/IOH = $\pm 2.6\text{mA}$ • 011 = IOL/IOH = $\pm 3.3\text{mA}$ • 100 = IOL/IOH = $\pm 6.1\text{mA}$ • 101 = IOL/IOH = $\pm 6.8\text{mA}$ • 110 = IOL/IOH = $\pm 8.5\text{mA}$ • 111 = IOL/IOH = $\pm 9.2\text{mA}$
3:2	GPIO2_PAD_CTRL[3:2]	0	R/W	Pad-programmable pull-up/pull-down control: • 00 = No pull-up or pull-down • 01 = Weak pull-down • 10 = Weak pull-up value 1 $\rightarrow 10\text{k}\Omega\text{--}35\text{k}\Omega$ • 11 = Weak pull-up value 2 $\rightarrow 130\text{k}\Omega\text{--}315\text{k}\Omega$
1	GPIO2_PAD_CTRL[1]	1	R/W	Pad output enable: • 0 = Pad is output-enabled • 1 = Pad is not output-enabled
0	GPIO2_PAD_CTRL[0]	0	R/W	Pad input enable: • 1 = Pad is input-enabled • 0 = Disables the pad input mode

GPIO3_PAD_CTRL—0x87**Table 226: GPIO3_PAD_CTRL—0x87**

Bits	Name	Default	R/W	Description
7	Reserved	0	-	Reserved.
6:4	GPIO3_PAD_CTRL[6:4]	0	R/W	Pad-programmable drive control—the following values are for the 3.3V VDDO: • 000 = IOL/IOH = $\pm 0.3\text{mA}$ • 001 = IOL/IOH = $\pm 1\text{mA}$ • 010 = IOL/IOH = $\pm 2.6\text{mA}$ • 011 = IOL/IOH = $\pm 3.3\text{mA}$ • 100 = IOL/IOH = $\pm 6.1\text{mA}$ • 101 = IOL/IOH = $\pm 6.8\text{mA}$ • 110 = IOL/IOH = $\pm 8.5\text{mA}$ • 111 = IOL/IOH = $\pm 9.2\text{mA}$
3:2	GPIO3_PAD_CTRL[3:2]	0	R/W	Pad-programmable pull-up/pull-down control: • 00 = No pull-up or pull-down • 01 = Weak pull-down • 10 = Weak pull-up value 1 $\rightarrow 10\text{k}\Omega\text{--}35\text{k}\Omega$ • 11 = Weak pull-up value 2 $\rightarrow 130\text{k}\Omega\text{--}315\text{k}\Omega$
1	GPIO3_PAD_CTRL[1]	1	R/W	Pad output enable: • 0 = Pad is output-enabled • 1 = Pad is not output-enabled
0	GPIO3_PAD_CTRL[0]	0	R/W	Pad input enable: • 1 = Pad is input-enabled • 0 = Disables the pad input mode

GPIO_OUT—0x88**Table 227: GPIO_OUT—0x88**

Bits	Name	Default	R/W	Description
7:4	Reserved	0	-	Reserved.
3	GPIO0_OUT[3]	0	R/W	Pad output data—the value that needs to be driven out on the GPIO3 pin.
2	GPIO0_OUT[2]	0	R/W	Pad output data—the value that needs to be driven out on the GPIO2 pin.
1	GPIO0_OUT[1]	0	R/W	Pad output data—the value that needs to be driven out on the GPIO1 pin.
0	GPIO0_OUT[0]	0	R/W	Pad output data—the value that needs to be driven out on the GPIO0 pin.

GPIO_IN—0x89**Table 228: GPIO_IN—0x89**

Bits	Name	Default	R/W	Description
7:4	Reserved	0	-	Reserved.
3	GPIO0_IN[3]	0	R	Pad input data—the value that is received on the GPIO3 pin.
2	GPIO0_IN[2]	0	R	Pad input data—the value that is received on the GPIO2 pin.
1	GPIO0_IN[1]	0	R	Pad input data—the value that is received on the GPIO1 pin.
0	GPIO0_IN[0]	0	R	Pad input data—the value that is received on the GPIO0 pin.

GPIO_INTR_CNTRL—0x8A**Table 229: GPIO_INTR_CNTRL—0x8A**

Bits	Name	Default	R/W	Description
7	Reserved	0	-	Reserved.
6	GP_RISE_EDGE [2]	0	R/W	Selects the interrupt mechanism for GPIO3. When setting this bit to 1, the hardware detects a rising edge transition on the GPIO3 input.
5	GP_RISE_EDGE [1]	0	R/W	Selects the interrupt mechanism for GPIO2. When setting this bit to 1, the hardware detects a rising edge transition on the GPIO2 input.
4	GP_RISE_EDGE [0]	0	R/W	Selects the interrupt mechanism for GPIO1. When setting this bit to 1, the hardware detects a rising edge transition on the GPIO1 input.
3	Reserved	0	-	Reserved.
2	GP_FALL_EDGE [2]	0	R/W	Selects the interrupt mechanism for GPIO3. When setting this bit to 1, the hardware detects a falling edge transition on the GPIO3 input.
1	GP_FALL_EDGE [1]	0	R/W	Selects the interrupt mechanism for GPIO2. When setting this bit to 1, the hardware detects a falling edge transition on the GPIO2 input.
0	GP_FALL_EDGE [0]	0	R/W	Selects the interrupt mechanism for GPIO1. When setting this bit to 1, the hardware detects a falling edge transition on the GPIO1 input.

GPIO_INTR_EN—0x8B**Table 230: GPIO_INTR_EN—0x8B**

Bits	Name	Default	R/W	Description
7:3	Reserved	0	-	Reserved.
2	GP_INTR_EN [2]	0	R/W	Enables the interrupt mechanism for GPIO3: 1 = Enables the interrupt 0 = Disables the interrupt
1	GP_INTR_EN [1]	0	R/W	Enables the interrupt mechanism for GPIO2: 1 = Enables the interrupt 0 = Disables the interrupt
0	GP_INTR_EN [0]	0	R/W	Enables the interrupt mechanism for GPIO1: 1 = Enables the interrupt 0 = Disables the interrupt

GPIO_INTR_STATUS—0x8C**Table 231: GPIO_INTR_STATUS—0x8C**

Bits	Name	Default	R/W	Description
7:3	Reserved	0	-	Reserved.
2	GP_INTR_STATUS [2]	0	R/W1C	Interrupt status for GPIO3—clears when writing a 1 to this register: 1 = Detects the event 0 = Event not detected
1	GP_INTR_STATUS [1]	0	R/W1C	Interrupt status for GPIO2—clears when writing a 1 to this register: 1 = Detects the event 0 = Event not detected
0	GP_INTR_STATUS [0]	0	R/W1C	Interrupt status for GPIO1—clears when writing a 1 to this register: 1 = Detects the event 0 = Event not detected

WAKE_D2D_PAD_CTRL—0x8D**Table 232: WAKE_D2D_PAD_CTRL—0x8D**

Bits	Name	Default	R/W	Description
7:4	Reserved	0	-	Reserved.
3	WAKE_D2D_PAD_CTRL[3]	0	R	Wake die to the die pad input status.
2	WAKE_D2D_PAD_CTRL[2]	0	R/W	Wake die to the die pad output value to be driven out from this pad if output enable is low (WAKE_D2D_PAD_CTRL[1]).
1	WAKE_D2D_PAD_CTRL[1]	1	R/W	Wake die to the die pad output enable (active low): 0 = Enables the pad output (value on WAKE_D2D_PAD_CTRL[2] is driven out) 1 = Disables the pad output
0	WAKE_D2D_PAD_CTRL[0]	0	R/W	Input enable for wake die to the die pad from Hudson: 1 = Enables the input pad 0 = Disables the pad input

I2S_PAD_CTRL2—0x8E**Table 233: I2S_PAD_CTRL2—0x8E**

Bits	Name	Default	R/W	Description
7	Reserved	-	-	Reserved.
6:5	RX_DATA_DCCTL	0	R/W	Pad-programmable pull-up/pull-down control for rx_data: 00 = No pull-up or pull-down 01 = Weak pull-down -> 130kΩ–450kΩ 10 = Weak pull-up value 1 -> 10kΩ–35kΩ 11 = Weak pull-up value 2 -> 130kΩ–315kΩ
4:2	TX_DATA_1_DRVCTL	0x7	R/W	Pad-programmable drive control for TX_DATA_1: 000 = IOL/IOH = ±0.3mA 001 = IOL/IOH = ±1mA 010 = IOL/IOH = ±2.6mA 011 = IOL/IOH = ±3.3mA 100 = IOL/IOH = ±6.1mA 101 = IOL/IOH = ±6.8mA 110 = IOL/IOH = ±8.5mA 111 = IOL/IOH = ±9.2mA
1:0	TX_DATA_1_DCCTL	0	R/W	Pad-programmable pull-up/pull-down control for TX_DATA_1: 00 = No pull-up or pull-down 01 = Weak pull-down -> 130kΩ–450kΩ 10 = Weak pull-up value 1 -> 10kΩ–35kΩ 11 = Weak pull-up value 2 -> 130kΩ–315kΩ

I2S_PAD_CTRL3—0x8F**Table 234: I2S_PAD_CTRL3—0x8F**

Bits	Name	Default	R/W	Description
7:5	RX_DATA_DRVCTL	0x7	R/W	Pad-programmable drive control for rx_data: • 000 = IOL/IOH = $\pm 0.3\text{mA}$ • 001 = IOL/IOH = $\pm 1\text{mA}$ • 010 = IOL/IOH = $\pm 2.6\text{mA}$ • 011 = IOL/IOH = $\pm 3.3\text{mA}$ • 100 = IOL/IOH = $\pm 6.1\text{mA}$ • 101 = IOL/IOH = $\pm 6.8\text{mA}$ • 110 = IOL/IOH = $\pm 8.5\text{mA}$ • 111 = IOL/IOH = $\pm 9.2\text{mA}$
4:2	TX_DATA_2_DRVCTL	0x7	R/W	Pad-programmable drive control for TX_DATA_2: • 000 = IOL/IOH = $\pm 0.3\text{mA}$ • 001 = IOL/IOH = $\pm 1\text{mA}$ • 010 = IOL/IOH = $\pm 2.6\text{mA}$ • 011 = IOL/IOH = $\pm 3.3\text{mA}$ • 100 = IOL/IOH = $\pm 6.1\text{mA}$ • 101 = IOL/IOH = $\pm 6.8\text{mA}$ • 110 = IOL/IOH = $\pm 8.5\text{mA}$ • 111 = IOL/IOH = $\pm 9.2\text{mA}$
1:0	TX_DATA_2_DCCTL	0	R/W	Pad-programmable pull-up/pull-down control for TX_DATA_2: • 00 = No pull-up or pull-down • 01 = Weak pull-down $\rightarrow 130\text{k}\Omega\text{--}450\text{k}\Omega$ • 10 = Weak pull-up value 1 $\rightarrow 10\text{k}\Omega\text{--}35\text{k}\Omega$ • 11 = Weak pull-up value 2 $\rightarrow 130\text{k}\Omega\text{--}315\text{k}\Omega$

IIR Filter Registers

IIR_COEFF_B0_LOW^{1,2}—0x90

Table 235: IIR_COEFF_B0_LOW^{1,2}—0x90

Bits	Name	Default	R/W	Description
7:0	B0[7:0]	0x00	R/W	IIR coefficient B0 lower byte.

IIR_COEFF_B0_HIGH^{1,2}—0x91

Table 236: IIR_COEFF_B0_HIGH^{1,2}—0x91

Bits	Name	Default	R/W	Description
7:0	B0[15:8]	0x00	R/W	IIR coefficient B0 higher byte.

IIR_COEFF_B1_LOW^{1,2}—0x92

Table 237: IIR_COEFF_B1_LOW^{1,2}—0x92

Bits	Name	Default	R/W	Description
7:0	B1[7:0]	0x00	R/W	IIR coefficient B1 lower byte.

IIR_COEFF_B1_HIGH^{1,2}—0x93

Table 238: IIR_COEFF_B1_HIGH^{1,2}—0x93

Bits	Name	Default	R/W	Description
7:0	B1[15:8]	0x00	R/W	IIR coefficient B1 higher byte.

IIR_COEFF_B2_LOW^{1,2}—0x94

Table 239: IIR_COEFF_B2_LOW^{1,2}—0x94

Bits	Name	Default	R/W	Description
7:0	B2[7:0]	0x00	R/W	IIR coefficient B2 lower byte.

IIR_COEFF_B2_HIGH^{1,2}—0x95

Table 240: IIR_COEFF_B2_HIGH^{1,2}—0x95

Bits	Name	Default	R/W	Description
7:0	B2[15:8]	0x00	R/W	IIR coefficient B2 higher byte.

IIR_COEFF_A1_LOW^{1,2}—0x96**Table 241: IIR_COEFF_A1_LOW^{1,2}—0x96**

Bits	Name	Default	R/W	Description
7:0	A1[7:0]	0x00	R/W	IIR coefficient A1 lower byte.

IIR_COEFF_A1_HIGH^{1,2}—0x97**Table 242: IIR_COEFF_A1_HIGH^{1,2}—0x97**

Bits	Name	Default	R/W	Description
7:0	A1[15:8]	0x00	R/W	IIR coefficient A1 higher byte.

IIR_COEFF_A2_LOW^{1,2}—0x98**Table 243: IIR_COEFF_A2_LOW^{1,2}—0x98**

Bits	Name	Default	R/W	Description
7:0	A2[7:0]	0x00	R/W	IIR coefficient A2 lower byte.

IIR_COEFF_A2_HIGH^{1,2}—0x99**Table 244: IIR_COEFF_A2_HIGH^{1,2}—0x99**

Bits	Name	Default	R/W	Description
7:0	A2[15:8]	0x00	R/W	IIR coefficient A2 higher byte.

COEFF_IIR_G^{1,2}—0x9A**Table 245: COEFF_IIR_G^{1,2}—0x9A**

Bits	Name	Default	R/W	Description
7:6	Reserved	-	-	Reserved.
5:4	COEFF_IIR	0x0	R/W	The IIR in the CX2081x is four-band. COEFF_IIR is used to set coefficients to a particular IIR: 0 = Writes coefficients to IIR0 1 = Writes coefficients to IIR1
3	Reserved	-	-	Reserved.
2:0	G	0x0	R/W	IIR gain value register G.

IIR_EN^{1,2}—0x9B**Table 246: IIR_EN^{1,2}—0x9B**

Bits	Name	Default	R/W	Description
7:4	Reserved	0x00	-	Reserved.
3	ADC4_IIR_EN	0x0	R/W	adc4_iir enable: 0 = Disables the IIR 1 = Enables the IIR
2	ADC3_IIR_EN	0x0	R/W	adc3_iir enable: 0 = Disables the IIR 1 = Enables the IIR
1	ADC2_IIR_EN	0x0	R/W	adc2_iir enable: 0 = Disables the IIR 1 = Enables the IIR
0	ADC1_IIR_EN	0x0	R/W	adc1_iir enable: 0 = Disables the IIR 1 = Enables the IIR

Note:

- The B0, B1, B2, A1, A2, and G IIR coefficients are readable back only before they are modified. When the coefficients are written to memory and changed for another biquad, the coefficients that are written for the previous biquad are not readable.
- The IIR clock needs to be present for the IIR coefficients to be written into memory. Before starting to write the IIR coefficients, enable the IIR clock gating.

COEFF_LATCH_EN—0x9C**Table 247: COEFF_LATCH_EN—0x9C**

Bits	Name	Default	R/W	Description
7:4	Reserved	0x00	-	Reserved.
3	COEFF_LATCH_EN_ADC4	0x0	R/W	When set, the coefficient latch starts for the IIR set in Table 245 on page 254 . This register is cleared when read with the control interface and the memory store is done.
2	COEFF_LATCH_EN_ADC3	0x0	R/W	When set, the coefficient latch starts for the IIR set in Table 245 on page 254 . This register is cleared when read with the control interface and the memory store is done.
1	COEFF_LATCH_EN_ADC2	0x0	R/W	When set, the coefficient latch starts for the IIR set in Table 245 on page 254 . This register is cleared when read with the control interface and the memory store is done.
0	COEFF_LATCH_EN_ADC1	0x0	R/W	When set, the coefficient latch starts for the IIR set in Table 245 on page 254 . This register is cleared when read with the control interface and the memory store is done.

ATT_SEL—0x9D**Table 248: ATT_SEL—0x9D**

Bits	Name	Default	R/W	Description
7:6	ATT_SEL_ADC4	0x0	R/W	Programmable ATT SEL for ADC4: • 00 = 0dB attenuation • 01 = –6dB attenuation • 10 = –12dB attenuation • 11 = –18dB attenuation
5:4	ATT_SEL_ADC3	0x0	R/W	Programmable ATT SEL for ADC3: • 00 = 0dB attenuation • 01 = –6dB attenuation • 10 = –12dB attenuation • 11 = –18dB attenuation
3:2	ATT_SEL_ADC2	0x0	R/W	Programmable ATT SEL for ADC2: • 00 = 0dB attenuation • 01 = –6dB attenuation • 10 = –12dB attenuation • 11 = –18dB attenuation
1:0	ATT_SEL_ADC1	0x0	R/W	Programmable ATT SEL for ADC1: • 00 = 0dB attenuation • 01 = –6dB attenuation • 10 = –12dB attenuation • 11 = –18dB attenuation Note: This is actually not attenuation, but giving room for the gain to adjust. If the gain is not adjusted and programmed as above, the output is seen as attenuated.

Analog ADC Control Registers

ANA_ADC1_CTRL_1—0xA0

Table 249: ANA_ADC1_CTRL_1—0xA0

Bits	Name	Default	R/W	Description
7	RX1_PGA_BYPASS	0	R/W	Channel 1 PGA bypass for the line-in mode: 0 = Does not bypass the PGA path 1 = Bypasses the PGA and routes the inputs directly into the AAF with 0dB gain
6	RX1_PGA_BYP_RCM	0	R/W	Channel 1 PGA common-mode input resistance shorting: 0 = Does not short the resistance 1 = Shorts the resistance to speed-up the capacitor charging
5:4	RX1_PGA_CTRL_RCM	0	R/W	Channel 1 high-gain PGA input impedance control: 0 = 500kΩ 1 = 250kΩ 2 = 125kΩ 3 = 25kΩ
3	RX1_PGA_MUTE	0	R/W	Channel 1 PGA mute control: 0 = PGA in normal mode 1 = Input pins are disconnected and PGA inputs are shorted to the bias
2	RX1_DSM_ENABLE	0	R/W	Channel 1 AAF and ADC enable: 0 = Shuts down the AAF and ADC 1 = Enables the AAF and ADC
1	RX1_PGA_ENABLE	0	R/W	Channel 1 PGA enable: 0 = Shuts down the PGA 1 = Enables the PGA
0	RX1_MICBIAS_ENABLE	0	R/W	Channel 1 micbias enable: 0 = Shuts down the micbias 1 = Enables the micbias

ANA_ADC1_CTRL_2—0xA1

Table 250: ANA_ADC1_CTRL_2—0xA1

Bits	Name	Default	R/W	Description
7:0	Reserved	0	-	Reserved.

ANA_ADC1_CTRL_3—0xA2**Table 251: ANA_ADC1_CTRL_3—0xA2**

Bits	Name	Default	R/W	Description
7:6	Reserved	0	-	Reserved.
5	RX1_ANA_CAL_EN	0	R/W	Places the channel 1 Rx into calibration mode: 0 = Normal operation 1 = Shorts the PGA inputs, reconfigures the AAF, and enables the comparator
4	RX1_INVERT_CLK	0	R/W	ADC clock polarity: 0 = Normal clocking for channel 1 DSM 1 = Invert clock going to channel 1 DSM
3	RX1_SEL_OUT_EDGE	0	R/W	ADC clocking edge: 0 = Channel 1 DSM output is clocked on the falling edge of the input clock 1 = Channel 1 DSM output is clocked on the rising edge of the input clock
2	RX1_DSM_DISABLE	0	R/W	ADC disable control (overrides the RX1_DSM_ENABLE register 0xA0 [2]): 0 = Normal operation 1 = Disables the DSM modulator for channel 1
1	RX1_VREFP_DISABLE	0	R/W	ADC disable the VREFP buffer (overrides the RX1_DSM_ENABLE register 0xA0 [2]): 0 = Normal operation 1 = Disables the VREFP buffer for channel 1
0	RX1_AAF_DISABLE	0	R/W	ADC disable control (overrides the RX1_DSM_ENABLE register 0xA0 [2]): 0 = Normal operation 1 = Disables the AAF for channel 1

ANA_ADC1_CTRL_4—0xA3**Table 252: ANA_ADC1_CTRL_4—0xA3**

Bits	Name	Default	R/W	Description
7:0	Reserved	0	-	Reserved.

ANA_ADC1_CTRL_5—0xA4**Table 253: ANA_ADC1_CTRL_5—0xA4**

Bits	Name	Default	R/W	Description
7:0	Reserved	0	-	Reserved.

ANA_ADC1_CTRL_6—0xA5**Table 254:** ANA_ADC1_CTRL_6—0xA5

Bits	Name	Default	R/W	Description
7:6	PGA_CTRL_TC	0	R/W	Controls mix of class AB for the tail current: • 0: – Class A = 16 cells – Class B = 88 cells • 1: – Class A = 24 cells – Class B = 80 cells • 2: – Class A = 40 cells – Class B = 64 cells • 3: – Class A = 104 cells – Class B = 0 cells
5:4	PGA_CTRL_RC	0	R/W	Linearization loop damping resistor: • 0 = 1.2kΩs (default setting) • 1 = 600Ωs • 2 = 300Ωs • 3 = 150Ωs
3:2	PGA_CTRL_I_LIN	0	R/W	NMOS linearization current density control: • 0 = 1X ~120μA (default setting) • 1 = 0.5X ~ 60μA • 2 = 4X ~480μA • 3 = 2X ~240μA
1:0	PGA_CTRL_I_IN	0	R/W	PMOS input current density control: • 0 = 1X ~120μA (Default setting) • 1 = 0.5X ~ 60μA • 2 = 4X ~480μA • 3 = 2X ~240μA

ANA_ADC1_CTRL_7—0xA6**Table 255: ANA_ADC1_CTRL_7—0xA6**

Bits	Name	Default	R/W	Description
7	PGA_CTRL_HI_Z	0	R/W	PGA high impedance control: 0 = Normal operation (default) 1 = Disconnects Rfnet from the operational amplifier (op-amp) (test)
6	PGA_CTRL_SHORT_RF	0	R/W	PGA short feedback resistance: 0 = Normal operation (default) 1 = Shorts-out Rfnet (test)
5:4	PGA_CTRL_VCM_VG	0	R/W	PGA common-mode virtual GND control: 0 = Track Vin signal level 1 = Reserved 2 = Reserved 3 = Reserved
3:0	PGA_CTRL_VCM_IN	0	R/W	PGA common-mode input voltage control: 0 = 1.254V 1 = 1.162V 2 = 1.208V 3 = 1.300V 4 = 1.347V 5 = 1.393V 6 = 1.439V 7 = 1.486V 8 = 1.532V 9 = 1.578V 10 = 1.624V 11 = 1.671V 12 = 1.717V 13 = 1.764V 14 = 1.811V 15 = 1.856V

ANA_ADC2_CTRL_1—0xA7**Table 256: ANA_ADC2_CTRL_1—0xA7**

Bits	Name	Default	R/W	Description
7	RX2_PGA_BYPASS	0	R/W	Channel 2 PGA bypass for line-in mode: 0 = Does not bypass the PGA path 1 = Bypasses the PGA and routes the inputs directly into the AAF with 0dB gain
6	RX2_PGA_BYP_RCM	0	R/W	Channel 2 PGA common-mode input resistance shorting: 0 = Does not short the resistance 1 = Shorts the resistance to speed-up the capacitor charging
5:4	RX2_PGA_CTRL_RCM	0	R/W	Channel 2 high-gain PGA input impedance control: 0 = 500kΩ 1 = 250kΩ 2 = 125kΩ 3 = 25kΩ
3	RX2_PGA_MUTE	0	R/W	Channel 2 PGA mute control: 0 = PGA in normal mode 1 = Disconnects the input pins and shorts the PGA inputs to the bias
2	RX2_DSM_ENABLE	0	R/W	Channel 2 AAF and ADC enable: 0 = Shuts down the AAF and ADC 1 = Enables the AAF and ADC
1	RX2_PGA_ENABLE	0	R/W	Channel 2 PGA enable: 0 = Shuts down the PGA 1 = Enables the PGA
0	RX2_MICBIAS_ENABLE	0	R/W	Channel 2 micbias enable: 0 = Shuts down the micbias 1 = Enables the micbias

ANA_ADC2_CTRL_2—0xA8**Table 257: ANA_ADC2_CTRL_2—0xA8**

Bits	Name	Default	R/W	Description
7:0	Reserved	0	-	Reserved.

ANA_ADC2_CTRL_3—0xA9**Table 258: ANA_ADC2_CTRL_3—0xA9**

Bits	Name	Default	R/W	Description
7:6	Reserved	0	-	Reserved.
5	RX2_ANA_CAL_EN	0	R/W	Places the channel 2 Rx into offset calibration mode: 0 = Normal operation 1 = Shorts the PGA inputs, reconfigures the AAF, and enables the comparator
4	RX2_INVERT_CLK	0	R/W	ADC clock polarity: 0 = Normal clocking for channel 2 DSM 1 = Invert the clock going to channel 2 DSM
3	RX2_SEL_OUT_EDGE	0	R/W	ADC clocking edge: 0 = Channel 2 DSM output is clocked on the falling edge of the input clock 1 = Channel 2 DSM output is clocked on the rising edge of the input clock
2	RX2_DSM_DISABLE	0	R/W	ADC disable control (overrides the RX2_DSM_ENABLE register 0xA7 [2]): 0 = Normal operation 1 = Disables the DSM modulator for channel 2
1	RX2_VREFP_DISABLE	0	R/W	ADC disable VREFP buffer (overrides the RX2_DSM_ENABLE register 0xA7 [2]): 0 = Normal operation 1 = Disables the VREFP buffer for channel 2
0	RX2_AAF_DISABLE	0	R/W	ADC disable control (overrides the RX2_DSM_ENABLE register 0xA7 [2]): 0 = Normal operation 1 = Disables the AAF for channel 2

ANA_ADC2_CTRL_4—0xAA**Table 259: ANA_ADC2_CTRL_4—0xAA**

Bits	Name	Default	R/W	Description
7:0	Reserved	0	-	Reserved.

ANA_ADC2_CTRL_5—0xAB**Table 260: ANA_ADC2_CTRL_5—0xAB**

Bits	Name	Default	R/W	Description
7:0	Reserved	0	-	Reserved.

ANA_ADC2_CTRL_6—0xAC**Table 261: ANA_ADC2_CTRL_6—0xAC**

Bits	Name	Default	R/W	Description
7	PGA_CTRL_IBOOST	0	R/W	Main PGA transconductor bias: 0 = Nominal—ib = 5μA (default) 1 = 20% boost—ib = 6μA
6	PGA_CTRL_IQCTRL	0	R/W	PGA op-amp output current: 0 = Output stage current 1X (default) 1 = Output stage current 2X
5:4	PGA_CTRL_OABIAS	0	R/W	PGA op-amp bias current adjustment: 100% 5μA (default) –25% –50% –50%
3	PGA_CTRL_CMLOOP_DISABLE	0	R/W	0 = Normal VG CM loop operation 1 = Turns off the VG CM loop (error correction)
2	PGA_CTRL_PDB_RIN	0	R/W	PGA input resistance: 0 = PGA input resistance is high-Z during the main PGA PDB 1 = Always connects the PGA input resistance
1:0	PGA_CTRL_PEAKDET	0	R/W	Peak detector decay slope (1x = slow, 10x = faster): - Tail current 1x, virtual GND 1x - Tail current 10x, virtual GND 1x - Tail current 1x, virtual GND 10x - Tail current 10x, virtual GND 10x

ANA_ADC2_CTRL_7—0xAD**Table 262:** ANA_ADC2_CTRL_7—0xAD

Bits	Name	Default	R/W	Description
7	AAF_LPMODE	0	R/W	1 = Enables the low-power mode for AAF.
6:4	AAF_STG2_IB_SEL	0	R/W	Control bias current for the AAF op-amp output stage: • 000 = 30μA • 001 = 33.75μA • 010 = 22.50μA • 011 = 26.25μA • 100 = 45μA • 101 = 48.75μA • 110 = 37.50μA • 111 = 41.25μA
3	AAFDSTM_IB_DIV2	0	R/W	1 = Enables the input bias current reduction by half for the AAF and DSM.
2:0	AAF_STG1_IB_SEL	0	R/W	Control bias current for the AAF op-amp input stage: • 000 = 5μA • 001 = 5.625μA • 010 = 3.750μA • 011 = 4.375μA • 100 = 7.5μA • 101 = 8.125μA • 110 = 6.250μA • 111 = 6.875μA

ANA_ADC3_CTRL_1—0xAE**Table 263: ANA_ADC3_CTRL_1—0xAE**

Bits	Name	Default	R/W	Description
7	RX3_PGA_BYPASS	0	R/W	Channel 3 PGA bypass for line-in mode: 0 = Does not bypass the PGA path 1 = Bypasses the PGA and routes the inputs directly into the AAF with 0dB gain
6	RX3_PGA_BYP_RCM	0	R/W	Channel 3 PGA common-mode input resistance shorting: 0 = Does not short the resistance 1 = Shorts the resistance to speed-up the capacitor charging
5:4	RX3_PGA_CTRL_RCM	0	R/W	Channel 3 high-gain PGA input impedance control: 0 = 500kΩ 1 = 250kΩ 2 = 125kΩ 3 = 25kΩ
3	RX3_PGA_MUTE	0	R/W	Channel 3 PGA mute control: 0 = PGA in normal mode 1 = Disconnects the input pins and shorts the PGA inputs to the bias
2	RX3_DSM_ENABLE	0	R/W	Channel 3 AAF and ADC enable: 0 = Shuts down the AAF and ADC 1 = Enables the AAF and ADC
1	RX3_PGA_ENABLE	0	R/W	Channel 3 PGA enable: 0 = Shuts down the PGA 1 = Enables the PGA
0	RX3_MICBIAS_ENABLE	0	R/W	Channel 3 micbias enable: 0 = Shuts down the micbias 1 = Enables the micbias

ANA_ADC3_CTRL_2—0xAF**Table 264: ANA_ADC3_CTRL_2—0xAF**

Bits	Name	Default	R/W	Description
7:0	Reserved	0	-	Reserved.

ANA_ADC3_CTRL_3—0xB0**Table 265: ANA_ADC3_CTRL_3—0xB0**

Bits	Name	Default	R/W	Description
7:6	Reserved	0	-	Reserved.
5	RX3_ANA_CAL_EN	0	R/W	Places the channel 3 Rx into offset calibration mode: 0 = Normal operation 1 = Shorts the PGA inputs, reconfigures the AAF, and enables the comparator
4	RX3_INVERT_CLK	0	R/W	ADC clock polarity: 0 = Normal clocking for channel 3 DSM 1 = Invert clock going to channel 3 DSM
3	RX3_SEL_OUT_EDGE	0	R/W	ADC clocking edge: 0 = Channel 3 DSM output is clocked on the falling edge of the input clock 1 = Channel 3 DSM output is clocked on the rising edge of the input clock
2	RX3_DSM_DISABLE	0	R/W	ADC disable control (overrides the RX3_DSM_ENABLE register 0xAE [2]): 0 = Normal operation 1 = Disables the DSM modulator for channel 3
1	RX3_VREFP_DISABLE	0	R/W	ADC disable VREFP buffer (overrides the RX3_DSM_ENABLE register 0xAE [2]): 0 = Normal operation 1 = Disables the VREFP buffer for channel 3
0	RX3_AAF_DISABLE	0	R/W	ADC disable control (overrides the RX3_DSM_ENABLE register 0xAE [2]): 0 = Normal operation 1 = Disables the AAF for channel 3

ANA_ADC3_CTRL_4—0xB1**Table 266: ANA_ADC3_CTRL_4—0xB1**

Bits	Name	Default	R/W	Description
7:0	Reserved	0	-	Reserved.

ANA_ADC3_CTRL_5—0xB2**Table 267: ANA_ADC3_CTRL_5—0xB2**

Bits	Name	Default	R/W	Description
7:0	Reserved	0	-	Reserved.

ANA_ADC3_CTRL_6—0xB3**Table 268: ANA_ADC3_CTRL_6—0xB3**

Bits	Name	Default	R/W	Description
7:6	Reserved	0	-	Reserved.
5:4	AAF_AIB_THRES	0	R/W	AAF input signal level for the variable bias current to get 95% bias current for the AAF op-amp output stage: 0 = -10dBFS 1 = -7dBFS 2 = -4dBFS 3 = -1.5dBFS
3	AAF_AIB_PD_FAST	0	R/W	Control peak detector slope for the variable bias current for the AAF op-amp output stage: 0 = 27V/s 1 = 240V/s
2:0	AAF_AIB_RANGE	0	R/W	Control fixed and variable portion of the bias current for the AAF op-amp output stage. The variable portion of the bias current is adaptively changed according to the AAF input signal level: 0 = 100% fixed/0% variable 1 = 87.5% fixed/12.5% variable 2 = 75% fixed/25% variable 3 = 62.5% fixed/37.5% variable 4 = 50% fixed/50% variable 5 = 37.5% fixed/62.5% variable 6 = 25% fixed/75% variable 7 = 12.5% fixed/87.5% variable

ANA_ADC3_CTRL_7—0xB4**Table 269: ANA_ADC3_CTRL_7—0xB4**

Bits	Name	Default	R/W	Description
7:6	DSM_COMP_IB_SEL	0	R/W	Control bias current for the DSM comparators: • 0 = 6.25μA • 1 = 7.50μA • 2 = 3.75μA • 3 = 5μA
5:4	DSM_OTA_CTRL	0	R/W	Control DSM first integrator op-amp that is composed of 10 parallel subunits: • 0 = 100% enabled • 1 = 80% enabled • 2 = 60% enabled • 3 = 40% enabled
3	DSM_LPMODE	0	R/W	1 = Enables the low-power mode for the DSM.
2:0	DSM_OTA_IB_SEL	0	R/W	Control bias current for the DSM integrator op-amps: • 0 = 6.250μA • 1 = 6.875μA • 2 = 7.500μA • 3 = 8.125μA • 4 = 3.750μA • 5 = 4.375μA • 6 = 5μA • 7 = 5.625μA

ANA_ADC4_CTRL_1—0xB5**Table 270: ANA_ADC4_CTRL_1—0xB5**

Bits	Name	Default	R/W	Description
7	RX4_PGA_BYPASS	0	R/W	Channel 4 PGA bypass for line-in mode: 0 = Does not bypass the PGA path 1 = Bypasses the PGA and routes the inputs directly into the AAF with 0dB gain
6	RX4_PGA_BYP_RCM	0	R/W	Channel 4 PGA common-mode input resistance shorting: 0 = Does not short the resistance 1 = Shorts the resistance to speed-up the capacitor charging
5:4	RX4_PGA_CTRL_RCM	0	R/W	Channel 4 high-gain PGA input impedance control: 0 = 500kΩ 1 = 250kΩ 2 = 125kΩ 3 = 25kΩ
3	RX4_PGA_MUTE	0	R/W	Channel 4 PGA mute control: 0 = PGA in normal mode 1 = Disconnects the input pins and shorts the PGA inputs to the bias
2	RX4_DSM_ENABLE	0	R/W	Channel 4 AAF and ADC enable: 0 = Shuts down the AAF and ADC 1 = Enables the AAF and ADC
1	RX4_PGA_ENABLE	0	R/W	Channel 4 PGA enable: 0 = Shuts down the PGA 1 = Enables the PGA
0	RX4_MICBIAS_ENABLE	0	R/W	Channel 4 micbias enable: 0 = Shuts down the micbias 1 = Enables the micbias

ANA_ADC4_CTRL_2—0xB6**Table 271: ANA_ADC4_CTRL_2—0xB6**

Bits	Name	Default	R/W	Description
7:0	Reserved	0	-	Reserved.

ANA_ADC4_CTRL_3—0xB7**Table 272: ANA_ADC4_CTRL_3—0xB7**

Bits	Name	Default	R/W	Description
7:6	Reserved	0	-	Reserved.
5	RX4_ANA_CAL_EN	0	R/W	Places the channel 4 Rx into offset calibration mode: 0 = Normal operation 1 = Shorts the PGA inputs, reconfigures the AAF, and enables the comparator
4	RX4_INVERT_CLK	0	R/W	ADC clock polarity: 0 = Normal clocking for the channel 4 DSM 1 = Inverts the clock going to the channel 4 DSM
3	RX4_SEL_OUT_EDGE	0	R/W	ADC clocking edge: 0 = Channel 4 DSM output is clocked on the falling edge of the input clock 1 = Channel 4 DSM output is clocked on the rising edge of the input clock
2	RX4_DSM_DISABLE	0	R/W	ADC disable control (overrides the RX4_DSM_ENABLE register 0xB5 [2]): 0 = Normal operation 1 = Disables the DSM modulator for channel 4
1	RX4_VREFP_DISABLE	0	R/W	ADC disable VREFP buffer (overrides the RX4_DSM_ENABLE register 0xB5 [2]): 0 = Normal operation 1 = Disables the VREFP buffer for channel 4
0	RX4_AAF_DISABLE	0	R/W	ADC disable control (overrides the RX4_DSM_ENABLE register 0xB5 [2]): 0 = Normal operation 1 = Disables the AAF for channel 4

ANA_ADC4_CTRL_4—0xB8**Table 273: ANA_ADC4_CTRL_4—0xB8**

Bits	Name	Default	R/W	Description
7:0	Reserved	0	-	Reserved.

ANA_ADC4_CTRL_5—0xB9**Table 274: ANA_ADC4_CTRL_5—0xB9**

Bits	Name	Default	R/W	Description
7:0	Reserved	0	-	Reserved.

ANA_ADC4_CTRL_6—0xBA**Table 275: ANA_ADC4_CTRL_6—0xBA**

Bits	Name	Default	R/W	Description
7:6	Reserved	0	-	Reserved.
5	DSM_DEMOFF	0	R/W	1 = Disables the DWA DEM for the multi-bit DAC in the DSM.
4	DSM_EN_DITHER	0	R/W	1 = Enables the pseudo random dither injection into the DSM.
3	DSM_CLKSEL	0	R/W	Selects the clock for the DSM: 0 = Digital clock 1 = PLL clock
2	DSM_VREFP_LPMODE	0	R/W	1 = Enables the low-power mode for the VREFP buffer.
1:0	DSM_VREFP_OUTCTRL	0	R/W	Controls the VREFP buffer strength: 00 = 100% 01 = 75% 10 = 50% 11 = 25%

ANA_ADC4_CTRL_7—0xBB**Table 276: ANA_ADC4_CTRL_7—0xBB**

Bits	Name	Default	R/W	Description
7:0	Reserved	0	-	Reserved.

ADC1_ANALOG_PGA—0xBC**Table 277: ADC1_ANALOG_PGA—0xBC**

Bits	Name	Default	R/W	Description
7:6	Reserved	0	-	Reserved.
5:1	RX1_ANALOG_PGA [5:1]	0	R/W	Channel 1 PGA settings: 0 = 0dB 1 = -6dB 2 = 3dB 3 = 3dB 4 = 4dB 5 = 5dB 6 = 6dB 7 = 7dB 8 = 8dB 9 = 9dB 10 = 10dB 11 = 11dB 12 = 12dB 13 = 13dB 14 = 14dB 15 = 15dB 16 = 16dB 17 = 17dB 18 = 18dB 19 = 19dB 20 = 20dB 21 = 21dB 22 = 22dB 23 = 23dB 24 = 24dB 25 = 25dB 26 = 26dB 27 = 27dB 28 = 28dB 29 = 29dB 30 = 30dB 31 = 30dB Refer to the "PGA" section in the <i>CX20810/CX20811 Data Sheet</i> for additional information on peak input level per gain setting.
0	RX1_ANALOG_PGA [0]	0	R/W	Channel 1 PGA 0.5dB step (implemented in AAF): 0 = 0.0dB 1 = 0.5dB

ADC2_ANALOG_PGA—0xBD**Table 278: ADC2_ANALOG_PGA—0xBD**

Bits	Name	Default	R/W	Description
7:6	Reserved	0	-	Reserved.
5:1	RX2_ANALOG_PGA [5:1]	0	R/W	Channel 2 PGA settings: 0 = 0dB 1 = -6dB 2 = 3dB 3 = 3dB 4 = 4dB 5 = 5dB 6 = 6dB 7 = 7dB 8 = 8dB 9 = 9dB 10 = 10dB 11 = 11dB 12 = 12dB 13 = 13dB 14 = 14dB 15 = 15dB 16 = 16dB 17 = 17dB 18 = 18dB 19 = 19dB 20 = 20dB 21 = 21dB 22 = 22dB 23 = 23dB 24 = 24dB 25 = 25dB 26 = 26dB 27 = 27dB 28 = 28dB 29 = 29dB 30 = 30dB 31 = 30dB Refer to the "PGA" section in the <i>CX20810/CX20811 Data Sheet</i> for additional information on peak input level per gain setting.
0	RX2_ANALOG_PGA [0]	0	R/W	Channel 2 PGA 0.5dB step (implemented in AAF): 0 = 0.0dB 1 = 0.5dB

ADC3_ANALOG_PGA—0xBE**Table 279: ADC3_ANALOG_PGA—0xBE**

Bits	Name	Default	R/W	Description
7:6	Reserved	0	-	Reserved.
5:1	RX3_ANALOG_PGA [5:1]	0	R/W	Channel 3 PGA settings: 0 = 0dB 1 = -6dB 2 = 3dB 3 = 3dB 4 = 4dB 5 = 5dB 6 = 6dB 7 = 7dB 8 = 8dB 9 = 9dB 10 = 10dB 11 = 11dB 12 = 12dB 13 = 13dB 14 = 14dB 15 = 15dB 16 = 16dB 17 = 17dB 18 = 18dB 19 = 19dB 20 = 20dB 21 = 21dB 22 = 22dB 23 = 23dB 24 = 24dB 25 = 25dB 26 = 26dB 27 = 27dB 28 = 28dB 29 = 29dB 30 = 30dB 31 = 30dB Refer to the "PGA" section in the <i>CX20810/CX20811 Data Sheet</i> for additional information on peak input level per gain setting.
0	RX3_ANALOG_PGA [0]	0	R/W	Channel 3 PGA 0.5dB step (implemented in AAF): 0 = 0.0dB 1 = 0.5dB

ADC4_ANALOG_PGA—0xBF**Table 280: ADC4_ANALOG_PGA—0xBF**

Bits	Name	Default	R/W	Description
7:6	Reserved	0	-	Reserved.
5:1	RX4_ANALOG_PGA [5:1]	0	R/W	Channel 4 PGA settings: 0 = 0dB 1 = -6dB 2 = 3dB 3 = 3dB 4 = 4dB 5 = 5dB 6 = 6dB 7 = 7dB 8 = 8dB 9 = 9dB 10 = 10dB 11 = 11dB 12 = 12dB 13 = 13dB 14 = 14dB 15 = 15dB 16 = 16dB 17 = 17dB 18 = 18dB 19 = 19dB 20 = 20dB 21 = 21dB 22 = 22dB 23 = 23dB 24 = 24dB 25 = 25dB 26 = 26dB 27 = 27dB 28 = 28dB 29 = 29dB 30 = 30dB 31 = 30dB Refer to the "PGA" section in the <i>CX20810/CX20811 Data Sheet</i> for additional information on peak input level per gain setting.
0	RX4_ANALOG_PGA [0]	0	R/W	Channel 4 PGA 0.5dB step (implemented in AAF) 0 = 0.0dB 1 = 0.5dB

Digital Test Registers

The following test registers are for device testing *only*, and should be treated as *Reserved*:

- DTEST0 0xC0
- DTEST1 0xC1
- DTEST2 0xC2
- DTEST3 0xC3
- DTEST4 0xC4
- DTEST5 0xC5

Coder-Decoder (CODEC) Test Registers

The following test registers are for device testing *only*, and should be treated as *Reserved*:

- CTEST0 0xD0
- CTEST1 0xD1
- CTEST2 0xD2
- CTEST3 0xD3
- CTEST4 0xD4
- CTEST5 0xD5
- CTEST6 0xD6
- CTEST7 0xD7
- CTEST8 0xD8
- CTEST9 0xD9
- CTEST10 0xDA
- CTEST11 0xDB

Status Registers

The following read status registers are for device testing *only*, and should be treated as *Reserved*:

CP_STATUS—0xE0

Table 281: CP_STATUS—0xE0

Bits	Name	Default	R/W	Description
7:5	Reserved	0	-	Reserved.
4:1	CP_STATUS [4:1]	0	R	CP test bus status from the analog can be read on the register.
0	CP_STATUS [0]	0	R	CP OK value read on the register.

PWM_STATUS—0xE1

Table 282: PWM_STATUS—0xE1

Bits	Name	Default	R/W	Description
7	Reserved	0	-	Reserved.
6:3	PWM_STATUS [6:3]	0	R	PWM test bus status from the analog can be read on this register.
2:0	PWM_STATUS [2:0]	0	R	PWM status from the analog can be read on this register.

MIC1_OFFSET_LSB_STATUS—0xE2

Table 283: MIC1_OFFSET_LSB_STATUS—0xE2

Bits	Name	Default	R/W	Description
7:0	MIC1_OFFSET_LSB	0	R	Channel 1 microphone path calibrated the value sent to the analog. The 8-bit LSB of 10-bit value is read here.

MIC1_OFFSET_MSB_STATUS—0xE3**Table 284: MIC1_OFFSET_MSB_STATUS—0xE3**

Bits	Name	Default	R/W	Description
7	MIC1_OFFSET_CAL_DONE	0	R	Status that indicates if the calibration is complete: 0 = One-time calibration did not complete 1 = One-time calibration is complete
6	MIC1_OFFSET_CAL_RUN_STATUS	0	R	Describes whether the microphone offset calibration engine is still calibrating: 0 = Calibration is inactive 1 = Calibration is in process
5:2	Reserved	0	R	Reserved.
1:0	MIC1_OFFSET [9:8]	2	R	Channel 1 microphone path calibrated value that is sent to the analog. The 2-bit LSB of 10-bit value is read here. The default 10-bit value: = 200 (hex) = 512 (dec) = –0 (sign mag)

MIC2_OFFSET_LSB_STATUS—0xE4**Table 285: MIC2_OFFSET_LSB_STATUS—0xE4**

Bits	Name	Default	R/W	Description
7:0	MIC2_OFFSET_LSB	0	R	Channel 2 microphone path calibrated value that is sent to the analog. The 8-bit LSB of 10-bit value is read here.

MIC2_OFFSET_MSB_STATUS—0xE5**Table 286: MIC2_OFFSET_MSB_STATUS—0xE5**

Bits	Name	Default	R/W	Description
7	MIC2_OFFSET_CAL_DONE	0	R	Status that indicates if the calibration is complete: 0 = One-time calibration did not complete 1 = One-time calibration is complete
6	MIC2_OFFSET_CAL_RUN_STATUS	0	R	Describes whether the microphone offset calibration engine is still calibrating: 0 = Calibration is inactive 1 = Calibration is in process
5:2	Reserved	0	-	Reserved.
1:0	MIC2_OFFSET [9:8]	2	R	Channel 2 microphone path calibrated value that is sent to the analog. The 2-bit LSB of 10-bit value is read here. The default 10-bit value: = 200 (hex) = 512 (dec) = –0 (sign mag)

MIC3_OFFSET_LSB_STATUS—0xE6**Table 287: MIC3_OFFSET_LSB_STATUS—0xE6**

Bits	Name	Default	R/W	Description
7:0	MIC3_OFFSET_LSB	0	R	Channel 3 microphone path calibrated value that is sent to the analog. The 8-bit LSB of 10-bit value is read here.

MIC3_OFFSET_MSB_STATUS—0xE7**Table 288: MIC3_OFFSET_MSB_STATUS—0xE7**

Bits	Name	Default	R/W	Description
7	MIC3_OFFSET_CAL_DONE	0	R	Status that indicates if the calibration is complete: 0 = One-time calibration did not complete 1 = One-time calibration is complete
6	MIC3_OFFSET_CAL_RUN_STATUS	0	R	Describes whether the microphone offset calibration engine is still calibrating: 0 = Calibration is inactive 1 = Calibration is in process
5:2	Reserved	0	-	Reserved.
1:0	MIC3_OFFSET [9:8]	2	R	Channel 3 microphone path calibrated value that is sent to the analog. The 2-bit LSB of 10-bit value is read here. Default 10-bit value: = 200 (hex) = 512 (dec) = –0 (sign mag)

MIC4_OFFSET_LSB_STATUS—0xE8**Table 289: MIC4_OFFSET_LSB_STATUS—0xE8**

Bits	Name	Default	R/W	Description
7:0	MIC4_OFFSET_LSB	0	R	Channel 4 microphone path calibrated value that is sent to the analog. The 8-bit LSB of 10-bit value is read here.

MIC4_OFFSET_MSB_STATUS—0xE9**Table 290: MIC4_OFFSET_MSB_STATUS—0xE9**

Bits	Name	Default	R/W	Description
7	MIC4_OFFSET_CAL_DONE	0	R	Status that indicates if the calibration is complete: 0 = One-time calibration did not complete 1 = One-time calibration is complete
6	MIC4_OFFSET_CAL_RUN_STATUS	0	R	Describes whether the microphone offset calibration engine is still calibrating: 0 = Calibration is inactive 1 = Calibration is in process
5:2	Reserved	0	-	Reserved.
1:0	MIC4_OFFSET [9:8]	2	R	Channel 4 microphone path calibrated value that is sent to the analog. The 2-bit LSB of 10-bit value is read here. Default 10-bit value: = 200 (hex) = 512 (dec) = –0 (sign mag)

System-on-a-Chip (SoC) Registers

DEVICE_ID—0xFC, 0xFD

Table 291: *DEVICE_ID—0xFC, 0xFD*

Bits	Name	Default	R/W	Description
15:0	DEVICE ID	0x0051	R	Device ID.

Revision ID/Stepping ID—0xFE

Table 292: *Revision ID/Stepping ID—0xFE*

Bits	Name	Default	R/W	Description
7:4	STEPPING ID	0	R	Stepping ID.
3:0	REVISION ID	1	R	Revision ID.

BOND_PAD_STATUS—0xFF

Table 293: *BOND_PAD_STATUS—0xFF*

Bits	Name	Default	R/W	Description
7:6	Reserved	0	-	Reserved.
5	BOND_PAD[5]	0	R	Reserved.
4	BOND_PAD[4]	0	R	Reserved.
3	BOND_PAD[3]	0	R	Reserved.
2	BOND_PAD[2]	0	R	Reserved.
1	BOND_PAD[1]	0	R	Reserved.
0	BOND_PAD[0]	0	R	Reserved.

The drawing illustrates a 16-pin Quad Flat Pack (QFP) package. The top view shows a square body with pins on all four sides. Key dimensions include a pin pitch of 0.050 inches (1.27 mm), a pin 1 corner radius of 0.005 inches (0.127 mm), and a body width of 0.400 inches (10.16 mm). The bottom view shows the underside of the package, including the exposed die attach pad and the lead thickness. The side view shows the package height and the seating plane. A table of mechanical specifications is provided, detailing parameters such as total thickness, stand-off, mold thickness, lead width, body size, lead pitch, ep size, lead length, package edge tolerance, mold flatness, coplanarity, lead offset, and exposed pad offset.

	SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS	A	0.8	0.85	0.9
STAND OFF	A1	0	0.035	0.05
MOLD THICKNESS	A2	---	0.65	0.67
L/F THICKNESS	A3		0.203 REF	
LEAD WIDTH	b	0.15	0.2	0.25
BODY SIZE	X D Y E		6 BSC 6 BSC	
LEAD PITCH	e		0.4 BSC	
EP SIZE	X J Y K	4.3 4.3	4.4 4.4	4.5 4.5
LEAD LENGTH	L	0.4	0.45	0.5
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.1	
COPLANARITY	ccc		0.08	
LEAD OFFSET	ddd		0.1	
EXPOSED PAD OFFSET	eee		0.1	

NOTES
1.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.

Figure 97: CX20810-11Z Package Dimensions—48-QFN

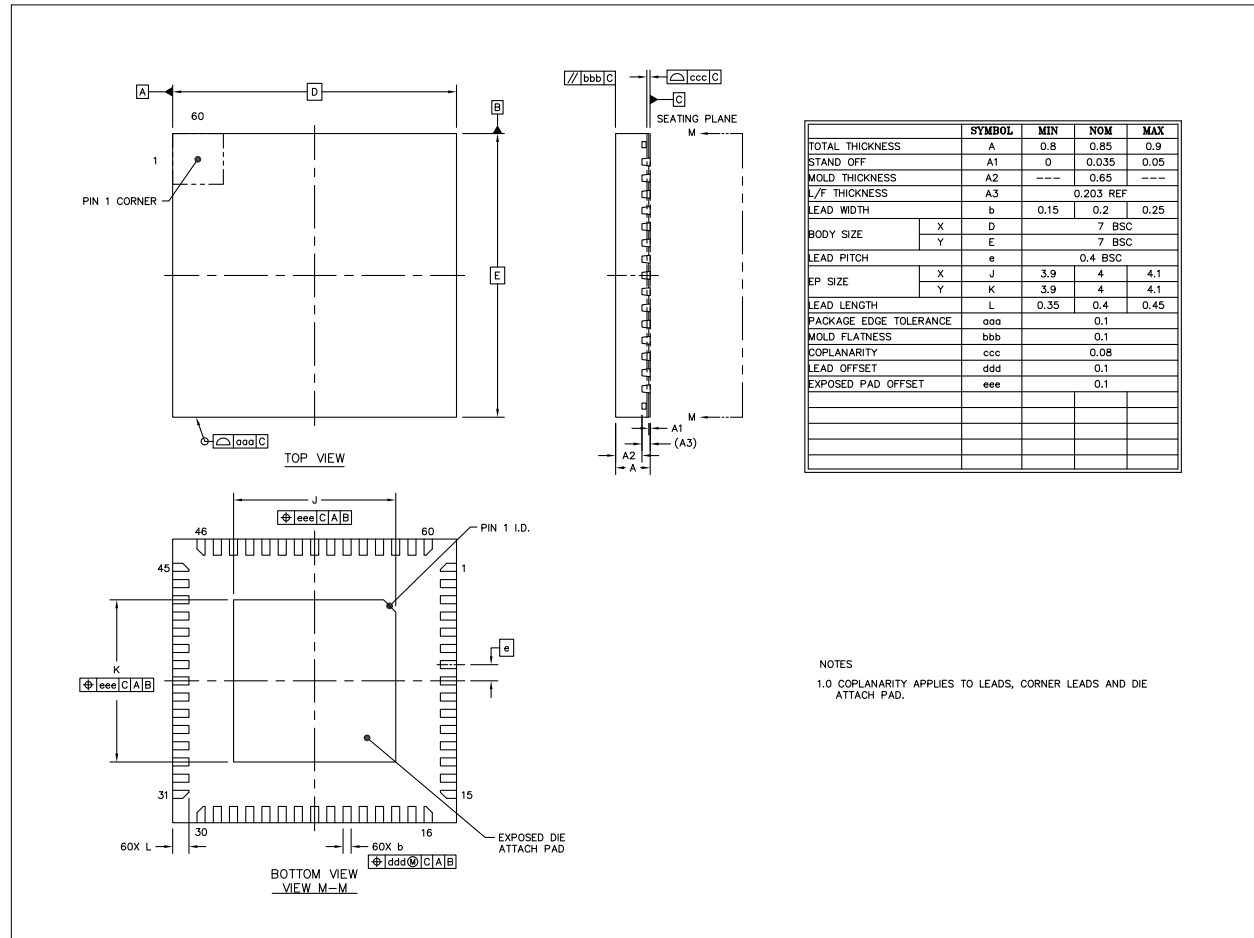


Figure 98: CX20811-11Z Package Dimensions—60-QFN

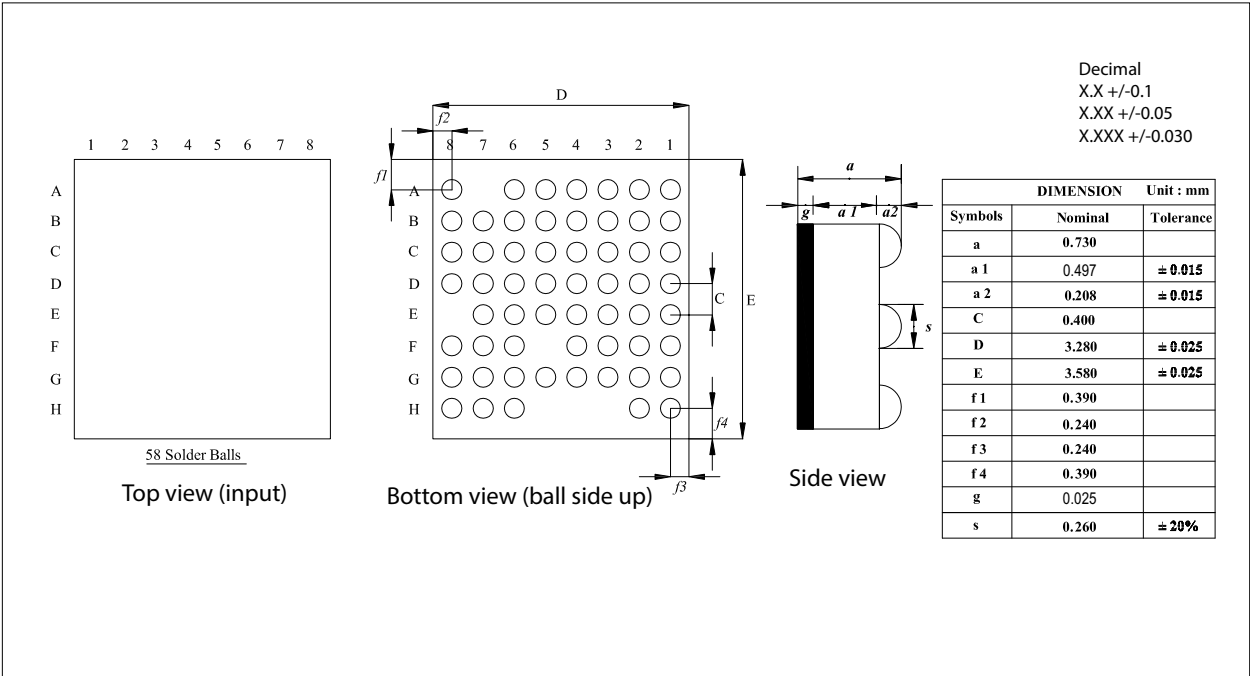


Figure 99: CX20811-15Z Package Dimensions—58-WLCSP

Package Thermal Data

Table 294: Package Thermal Data

Item	Value	
48-QFN	Θ_{ja} (°C/W)	28.7
	Θ_{jc} (°C/W)	11.6
60-QFN	Θ_{ja} (°C/W)	29.3
	Θ_{jc} (°C/W)	11.4
58-WLCSP	Θ_{ja} (°C/W)	65.7
	Θ_{jc} (°C/W)	3.7

Table 295: Test Board and Conditions for Thermal Data

Item	QFN Value	WLCSP Value
Size (in mm)	76.2 x 114.3	101.5 x 114.5
Motherboard Thickness (in mm)	1.6	1.6
Motherboard Material	FR-4	FR-4
Number of Layers in Motherboard	4	4

Ordering Information

The following table lists the ordering information.

Table 296: Ordering Information

Part Number	Description	Package
CX20810-11Z	4-channel Input	48-pad QFN, 6mm x 6mm
CX20811-11Z	4-channel Input with Playback Digital PWM Class-D Amp	60-pad QFN, 7mm x 7mm
CX20811-15Z	4-channel Input with Playback Digital PWM Class-D Amp	58-ball, WLCSP, 3.280mm x 3.580mm

Note:

- All devices are lead-free and RoHS, as established by JIG-101 Ed 4.1:
 - 2002/95/EC (RoHS)
 - 2011/65/EU (RoHS2)
 - SJ/T 11363—2006 (China RoHS)
 - PFOS compliant (2006/122/EC)
- Halogen/BFR/PC compliant

The devices in this publication are lead-free (Pb-Free) and China RoHS compliant . Contact the local Synaptics sales office for advanced software options.

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